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Performance Analysis of Different Level D-Statcom using Finfet Technology

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Abstract:

Due to scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) with each new generation of CMOS technology has provided us with improved circuit performance and cost per function over several decades. But, continued transistor scaling will not bestraightforward in the sub-32 nm regime because of fundamental materialand process technology limits. The main challenges in this regime are twofold: (a) minimization of leakage current (subthreshold and gate leakage), and (b) reduction in the device-to-device variability to increase yield.

FinFET's enhanced channel characteristics more than double energy efficiency gains contrast to current planarnodes also FinFETfacilitates gate control on multiple sides of the fin, which progresses electrostaticcontrol. The projectedideapermitsthe recompense thereactive power by absorbing/producinga currentflowcorrespondentto the essentialreactive powerbetter than

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

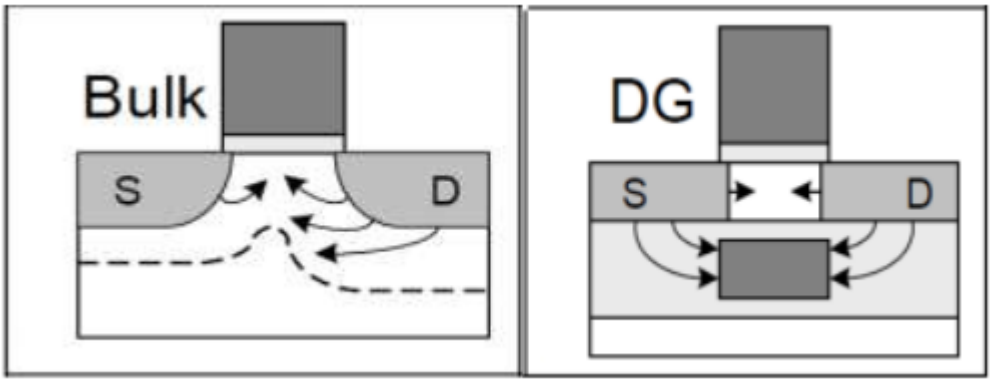
the existing IEEE HVDC 30-Bus System. The recitalof the anticipatedmodelis simulated in MATLAB environment.

KeyWords: FinFET, STATCOM, phase current

Introduction:

Transmission methods showcontinuous changes in hasty reconstruction across worldwide. The operating mode is initiated newly with the profound load is under consideration. As well, most loads are unbalanced or non-linear. Higher amount of quality problem is encountered in the power systems consequently such as harmonics current burden, extreme neutral current, high reactive power poor voltage regulation etc. Numerous methods and proceduresare accomplishedto suppress the power quality problem across the country.

A large number of recent works suggest that double gate (DG) devices are the best alternatives. Among the various types of DG devices, quasi-planar FinFETiseasier to manufacture compared to planar double gatedevices. FinFETs employ very thin undoped body to suppress subsurface leakage paths and, hence, reduced SCEs. An undoped or lightly doped body eliminates threshold voltage (Vt) variations due torandom dopant fluctuations and enhances carrier transportresulting in higher on current.As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the “short-channel effects” start plaguing MOSFETs.



Encroachment Of Electric Field Lines From Source And Drain On The Channel Region A: Bulk MOSFET; B: Double-Gate MOSFET

MOSFET TECHNOLOGY:

Metal-Oxide Semiconductor Field-Effect Transistor or simply called MOSFET is another type of transistor besides Bipolar Junction Transistor (BJT). The first MOSFETis invented by Kahng and Atalla in 1960 which contribute to cost-effective for a large number of transistors

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

on a single silicon chip compared to BJT. MOSFET is a four terminal device (drain, source, gate and bulk) where the amount of current flows between source and drain terminals is determined from the voltage applied to the gate terminal.

RELATED WORK:

Power quality problem is an occurrence manifested as a nonstandard voltage, current or frequency that results in a failure or a miss-operation of end user equipment.DSTATCOM is a shunt-connected custom power device specially designed for power factor correction, current harmonics filtering and loadbalancing. It is often referred to assome cases:

(a)WhenDSTATCOM is connected to weak supply system for power factor correction and load balancing.

(b)Non-linear load generated harmonics DSTATCOM current balance these unbalanced load current.

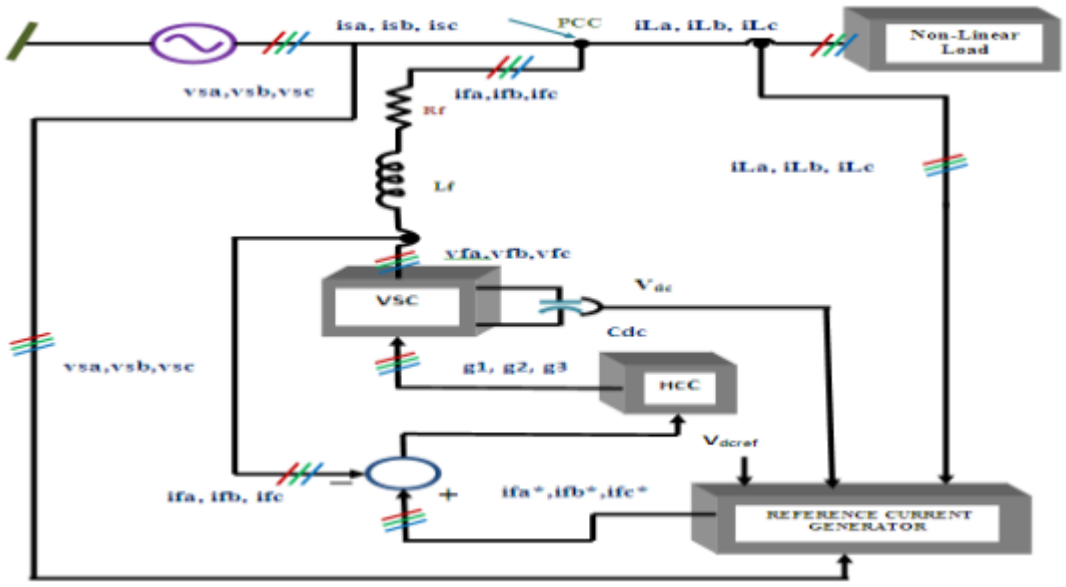
(c)When three phase uncontrolled diode bridge rectifier with its dc bus,it gives the transient response of distribution system with DSTATCOM for supply voltage and supply current.

(d)When unbalanced, three phase,non-linear load is connected source current are balanced and sinusoidal.

SYSTEM CONFIGURATION:

Figure below shows the basic circuit diagram of a D-STATCOM system with non -linear load connected three phase three wire distribution system.A nonlinearload is realized by using a three phasefull bridge diode rectifier. A three phase voltage source converter (VSC) working as a D-STATCOM is realized using six insulated gate bipolar transistor (IGBTs) with anti-parallel diodes.

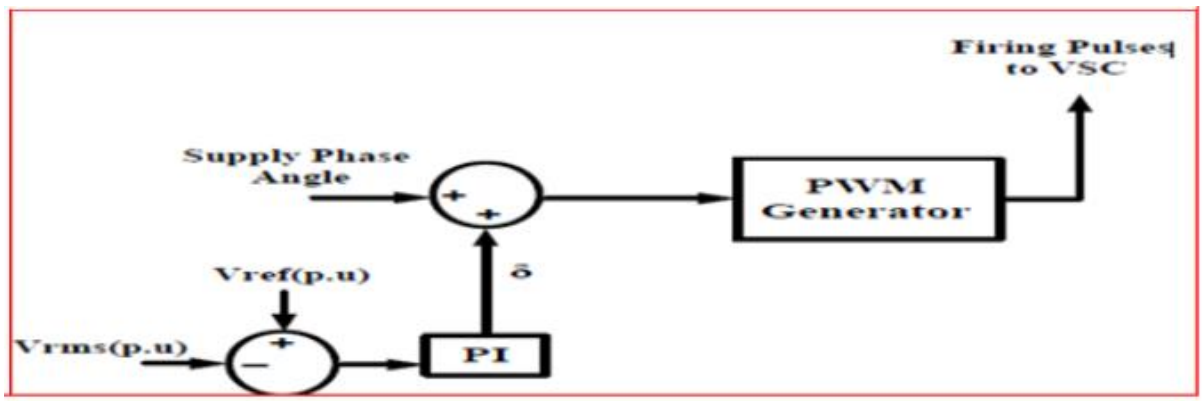
ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019



System Design of D-STATCOM

Controller:

The main Aim of the control scheme is to maintain constant voltage magnitude at the point wherea sensitive load is connected under system is in disturbances. In this control algorithm the voltage regulation is achieved in a DSTATCOM by themeasurement of the RMS voltage at the load point and no requirements of reactive power measurements.



PI Controller

Results and Discussion:

To investigate the performance of the D-STATCOM for p-q control algorithm, simulations are performed on matlabplatform . A three phase three wire distribution system with parameters given belowis considered for simulation.The performance of the control algorithm isevaluated based on two different cases.

System Parameters:

Supply voltage:50Vrms (L-N), 50Hz, three phase balanced

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

Source impedance:Rs=0.1Ω, Ls=.5mH

Nonlinear load: Three phase full bridge diode rectifier with load (L=10mH, RL=3.7Ω)

DC storage Capacitor Cdc=2000μF

Interface inductor Lf=2.2mH, Rf=0.1Ω

DC Link voltage Vdc=100V

Case1-BalancedSource and balanced Non-Linear load

Case2-Balanced Source andUnbalanced Non-linear load.

SIMULATION

Case-1

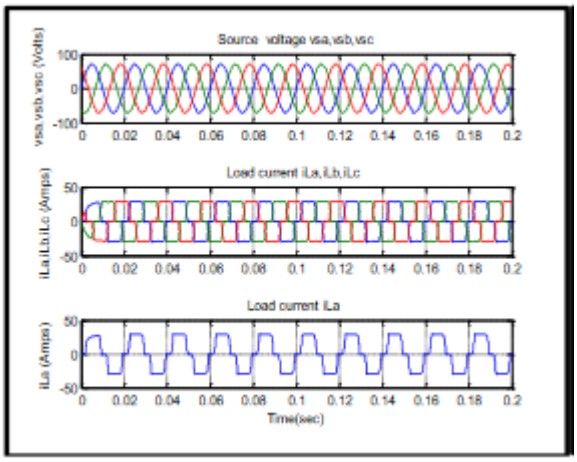


Fig: a. balancedsource voltage,Loadcurrent, Load currentPhase A

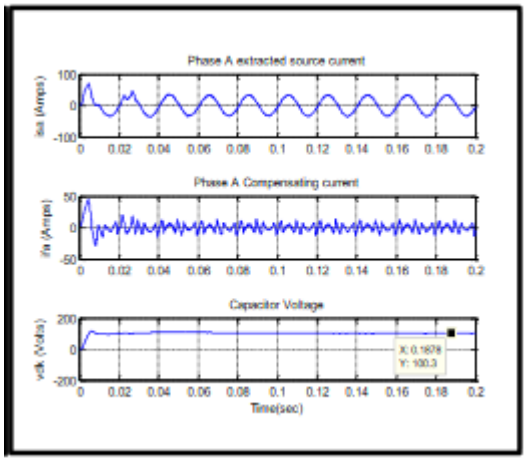


Fig: bPhase A extracted Source current, Compensating current, DC link Capacitor Voltage

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

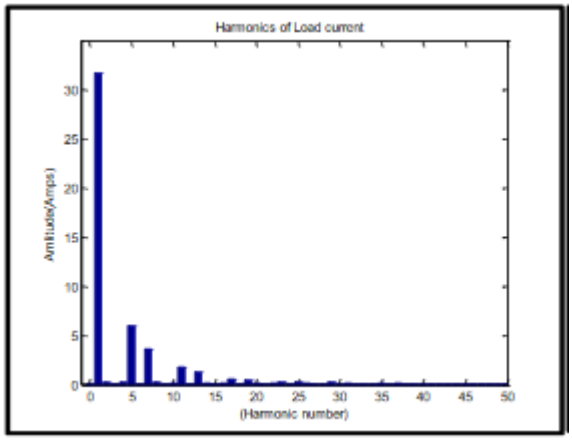


Fig: c Harmonics of Load currentof Phase A

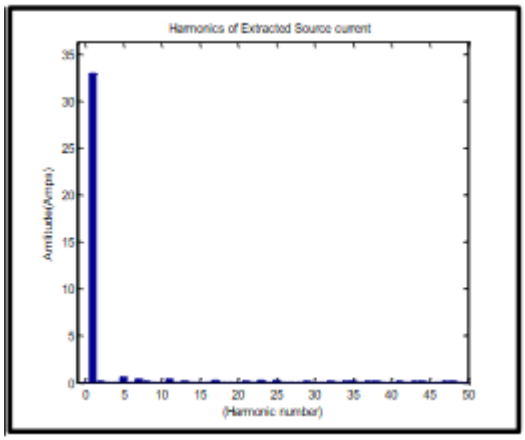


Fig: d Harmonics of extracted Source currentof phase A

Case-2

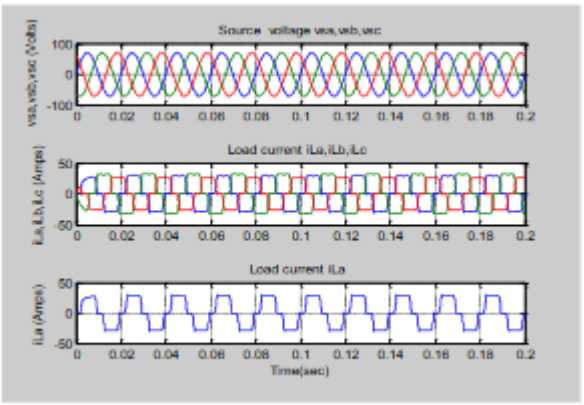


Fig: a balancedsource voltage,Unbalanced Load current,Load currentPhase

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

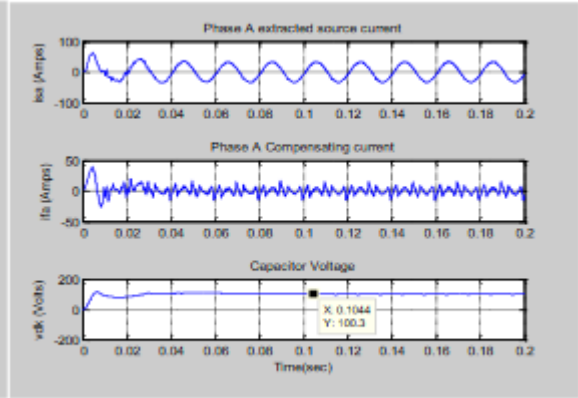


Fig b: Phase A extracted Source current, compensating currentand DC link Capacitor Voltage

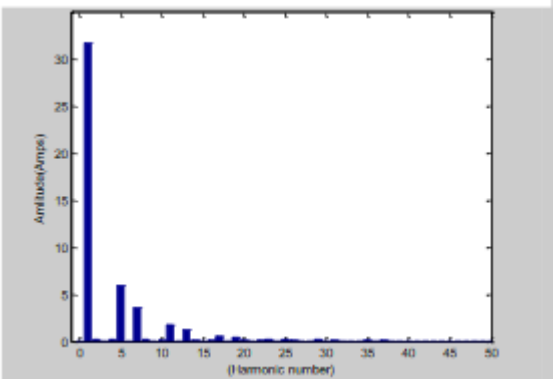


Fig c: Harmonics of Load currentof Phase A

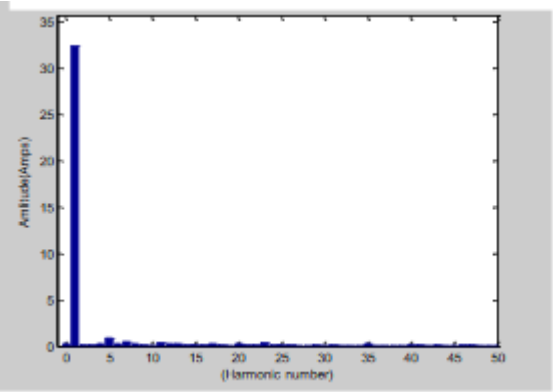


Fig d: Harmonics of extracted Source currentof phase A

Case-1

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

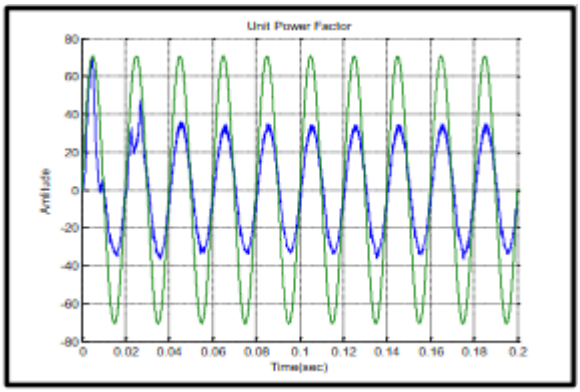


Fig: a case 1 power factor

Case: 2

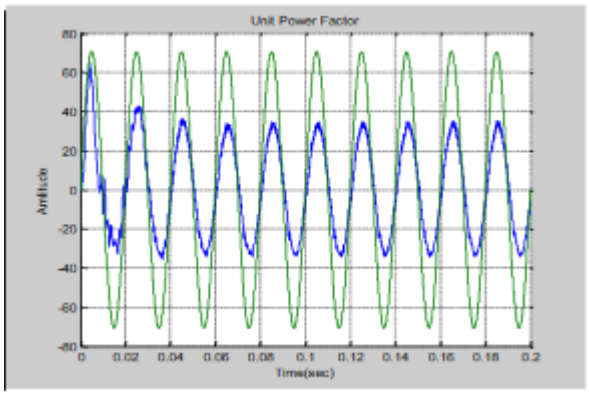


Fig b: case 2 power factor

After the simulation we get some unbalance waveform when RLC load is connected and DSTATCOM is not responding at this time

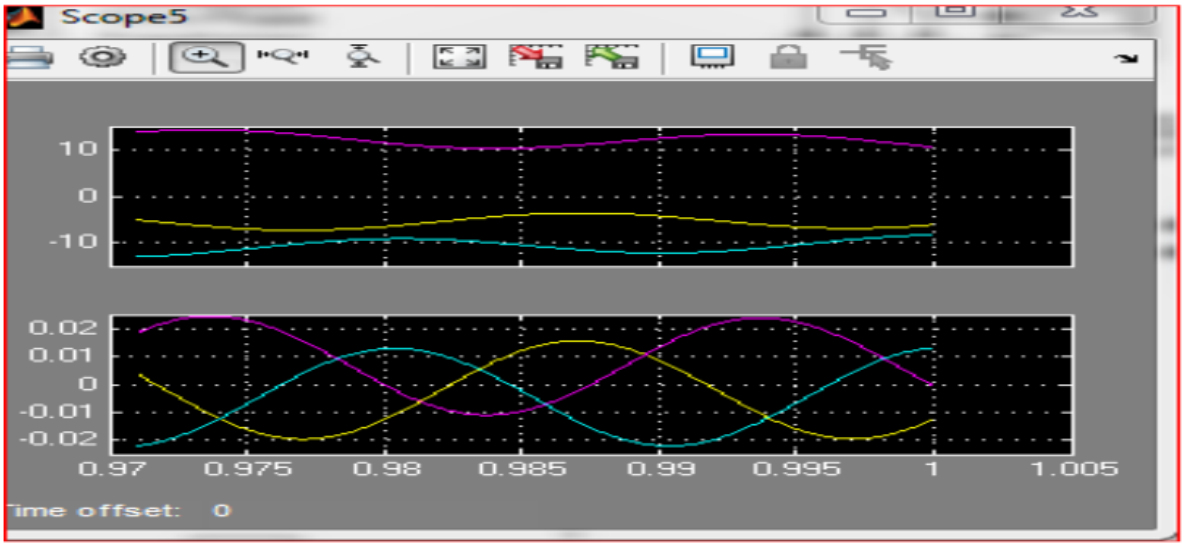


Fig: Response of unbalance load (RLC)

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

The second simulation was performed when RC load is connectedand DSTATCOM is not responding.

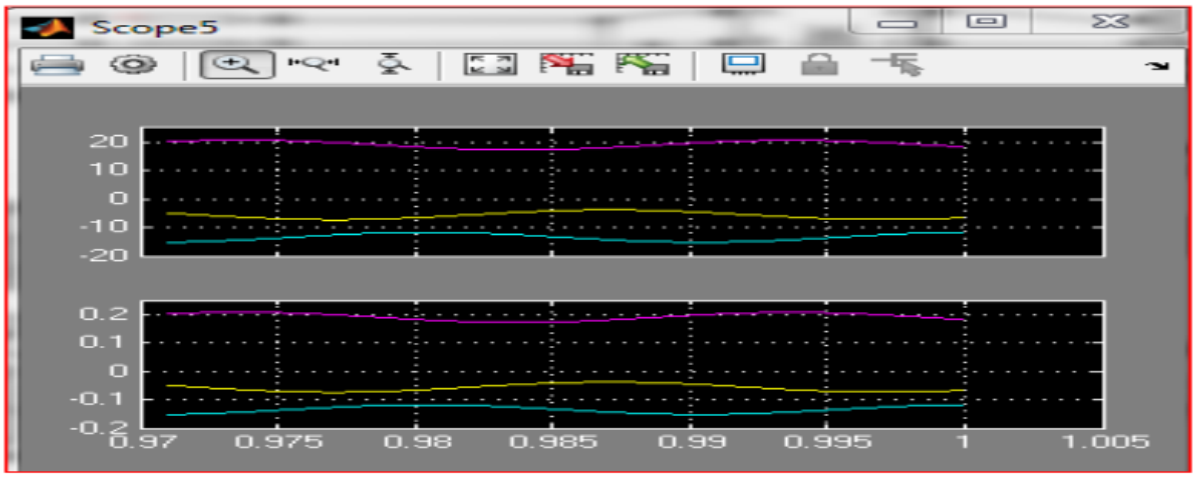


Fig: Response with unbalanced load(RC)

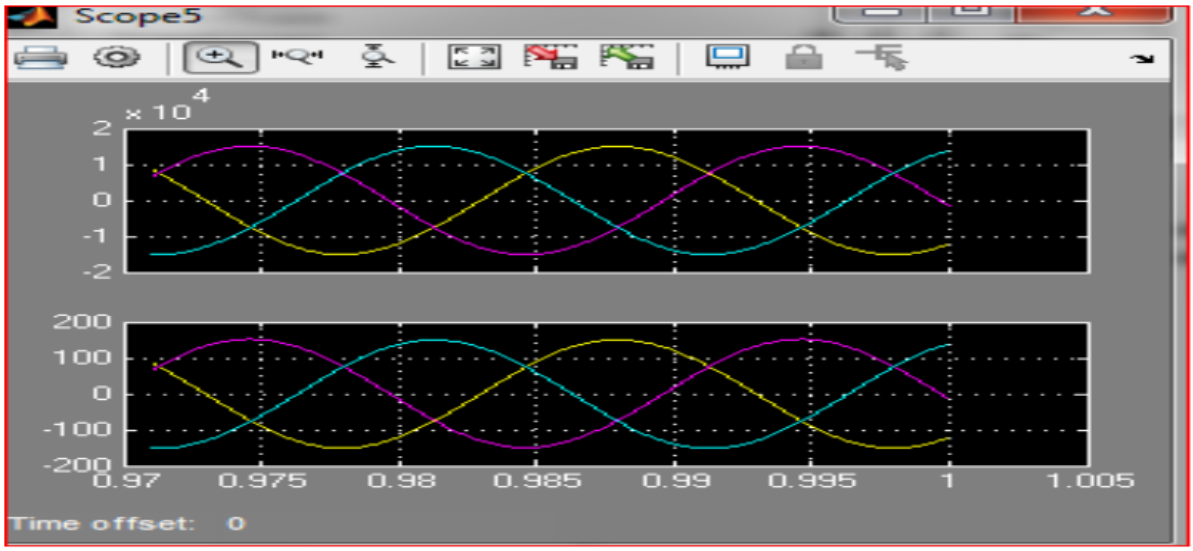


Fig: Response after DSTATCOM connection

Conclusion:

High-qualityHVDC design begins with a comprehensiveunderstanding of the essentialideas,and operation and control of HVDC method. There are many bases for operation and control before acting on them, but for High voltage direct current (HVDC) transmission there are numerousrestrictions. Thereforeit is essentialto test the systems for diversecondition, and inspectingthe system for boundedviolations by means ofcharacteristicsof Power Flow. The highly developed graphic facilities available in MATLAB/Simulink were used to conduct all aspects of model implementation and to carry out extensive simulation studies in the developed test systems. Different loads has been tested

ISSN: 0976-5425
Vol-5-Issue-4-July-August-2019

in the system and finally it can be concluded that there may be distortion in the voltage and current wave form due to application of unbalanced load or single phase load. This distorted waveform can be improved by connecting DSTATCOM. DSTATCOM is an efficient tool for mitigation of power quality issue.

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