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FPGA Based Reconfiguration Procedure Adopted To Obtain Secured Images

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Abstract:

The main focus of the proposed work is to obtain secured images using reconfigurable FPGA (Field Programmable Gate Array) based applications. Reconfigurable devices offer both the flexibility of computer software and the ability to design custom high performance computing circuits. The high performance image filters on FPGA will reduce evolution time. The proposed work exploits the inherent parallelism to obtain robust and secured images with the help of FPGA based reconfigurable procedure.

Keywords:

CLB, Combinational Logic Circuit, image filters, reconfiguration, area utilization,

Introduction:

By exploring large design search space, the CLB(Configurable Logic Blocks) scheme adapted to changes in task requirement or environment through its ability to reconfigure its own structure online and autonomously. The CLB architecture for image enhancement compensated uniformly for both slow and rapid SNR changes. In the recent developments, deterministic polynomial time algorithms are used to obtain secured shared resources. The proposed work exploits the inherent parallelism to obtain robust and secured images.

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Most of the image processing algorithms are time consuming due to large amount of calculations involved in them. Hence it is desirable to use high speed system. The most effective solution is to use FPGA. Single FPGA can perform single image processing algorithm at a time. Hence to make it multitasking the option of reconfigurability can be used. FPGA systems can work with speed comparable to ASIC (Application Specific Integrated Circuit) and with much more flexibility. Once a FPGA system is configured, it acts as ASIC system. This limits to perform various types of applications with the speed of FPGA. This problem can be solved by configuring FPGA again and again. In this way we increase flexibility of FPGA. Reconfigurable custom computing machines, implemented as arrays of FPGAs, have been successfully used to accelerate applications executing on PCs or workstations.

Literature Survey:

Sancho et al proposed two evolutionary programming algorithms which have the minimum values of objective functions. The designed prototype filters are only suitable to obtain near perfect reconstruction filter banks.

Jin Wing, Chang Hao Piao and Chang Ho Lee proposed a multi virtual reconfigurable circuit to evolve combinational logic circuits in parallel. The core idea behind this work is to divide a combinational logic circuit into several multiple circuits.

Sekanina developed a design procedure of image filters with virtual reconfigurable circuits. Digital image processing operations like image detection, smoothing, image compression have been carried out with this procedure. This work presents a reliable procedure for implementing

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high performance image filters on FPGA. Sekanina's procedure is a best compromise between software and hardware solutions.

Lukas Sekanina and Petr Mikusek proposed three instances of a reconfigurable circuit and analysed their properties with the help of brute force and evolutionary algorithms.

Novel circuit architecture for FPGA image filter evolution is proposed in Zden ek Vasicek and Lukas Sekanina. Karel Slany and Sekanina work analyses fitness landscapes for the image filter design problem using functional level Cartesian Genetic Programming.

Jie Li and Shitan Haung proposed a two stage adaptive noise removal scheme which includes noise detection and noise cancellation.

Proposed Work:

RECONFIGURABLE TECHNIQUES

1. Complete Reconfiguration

In this type of reconfiguration, FPGA can be configured with a single configuration code at a time. In order to change functionality of system, configuration code needs to be changed. Configuration can be done by serial or parallel communication. Computers, microcontrollers can be used as master devices. In computer based configuration, communication can be carried out using RS232 or USB port for serial communication.

2. Partial Reconfiguration

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Run time partial reconfiguration is useful to designers who want to develop applications demanding adaptive and flexible hardware. Using partial reconfiguration can result in power and area savings. But an intelligent system is needed to manage reconfiguration in order to save power and meet timing constrains in real time systems.

Results:

This application is used to perform area utilization results on system architecture

Module	FFs	LUT	BRAM
Multicre Interconnect	8825	8865	0
Gather	576	727	9
AXI Interconnect	232	233	0
Reset Processing System	54	49	0

The above results shows area results of system architecture using Xilinx and proves that the cost of incorporating software-driven control and management is marginal.

Conclusion:

The implementation results show that platform's adaptability and flexibility come at the cost of area where, significant amount is consumed by the interconnect followed by software-controlled distribution of window of pixel

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