

Normally OFF III-V Gate All Around FET For Analog Applications

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Abstract: In this paper, a new structure of III-V FET, gate all around FET is presented. Normally III-V FET is in ON state and operates in depletion mode with negative value of threshold voltage. The negative threshold voltage is due to higher inversion charge at the heterointerface due to polarization charges and discontinuity in the conduction band. The presented model in this work can successfully operate in enhancement mode and provides positive threshold voltage by reducing polarization charges at the heterointerface of AlGa_N barrier and Ga_N buffer layer. The proposed device can be used in the electronic applications where the demand of minimum power dissipation and minimum leakage current is on highest priority.

Keywords: III-V; FET; threshold voltage; AlGa_N; Ga_N

1. Introduction:

Si based devices have been extensively used since past, but due to lower energy band gap these devices cannot be used for applications where there is requirement of higher breakdown voltage [1]. In addition to it, Si based devices are limited to lower frequency applications, but where higher frequency is needed than novel semiconductor materials are required [2], [3]. In addition to it, wide band gap devices are more thermally stable and possess lower ON resistance in comparison to narrow bandgap semiconductor materials, but at the cost of more leakage in the device. Earlier, GaAs devices were extensively used, but these devices provide lower inversion charge at the heterointerface due to the diffusion of charge carriers from the wide bandgap barrier layer to the lower bandgap buffer layer [4]. Ga_N based devices having wide energy bandgap are exploited popularly in the today's electronics market. These devices have wide energy band gap than Si and GaAs based devices [5]. The unique transport mechanism of the transfer of charge carriers from wide energy bandgap material to the narrow bandgap material due to diffusion in III-V based devices makes them normally ON with negative threshold voltage. Consequently, leakage current is increased due to higher gate current and results in higher power dissipation. In order to reduce the power dissipation, the device needs to operate in enhancement mode. The novel gate all around structure successfully makes the III-V FET device to operate in enhancement mode and provide positive threshold voltage and the proposed III-V device can be used in the electronic applications where lower power dissipation is required, thus improving the limitations of Si devices [6]-[7].

2. Model description:

Fig. 1 represents the structure of III-V gate all around FET. The gate electrode is wrapped all around the barrier layer. The undoped AlGa_N barrier layer thickness is 2 nm and the atomic composition of Aluminium is 0.30.

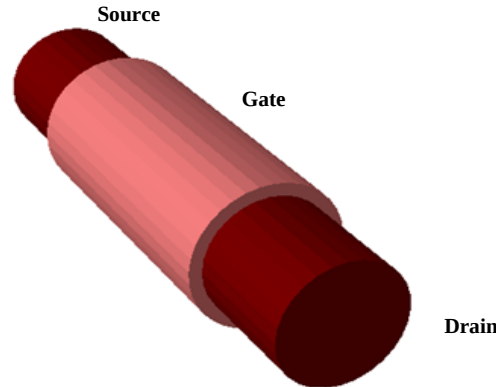


Fig. 1: Structure of III-V Gate all around FET (AlGa_N layer coated on Ga_N)

3. Results and discussions:

A vertical cut-line at the heterointerface of AlGa_N and Ga_N is introduced in the structure having barrier layer thickness of 2 nm and atomic composition of Al as 0.3. The conduction and valence band energy diagrams of the present model w.r.t. gate voltage and fixed drain voltage ($V_D=0$ V) are represented by Fig. 2(a-c). V_G is varied as 0, 0.5, and 1 V. It is evident from Fig. 2(a-c) that Fermi energy level approaches towards conduction band with increased gate voltage.

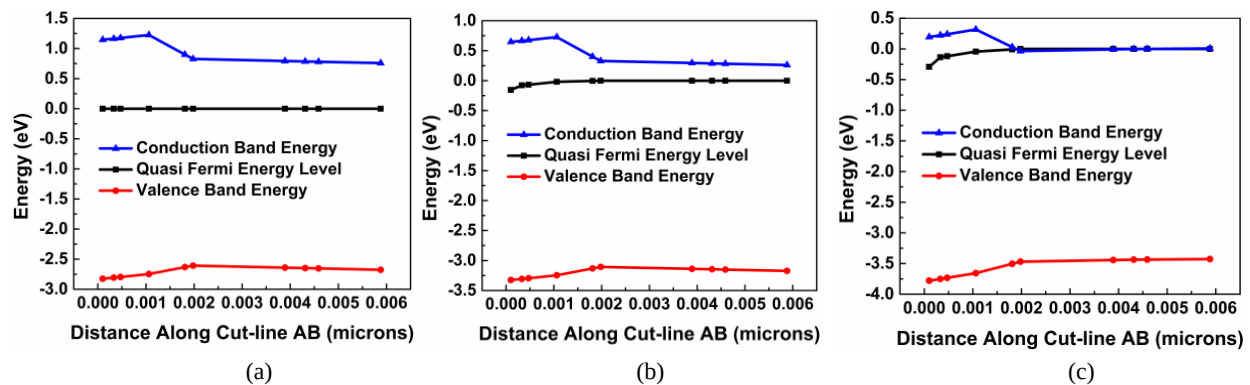


Fig. 2: Energy Band Diagram at $V_D=0$ V (a) $V_G=0$ V (b) $V_G=0.5$ V (c) $V_G=1$ V

The potential contour w.r.t. V_G and for $V_D=0$ V is represented by Fig. 3(a-c). The V_G is varied as 0, 0.5, and 1V and V_D is kept fixed at 0 V. The inversion charge at the heterointerface increases with increase in applied gate voltage.

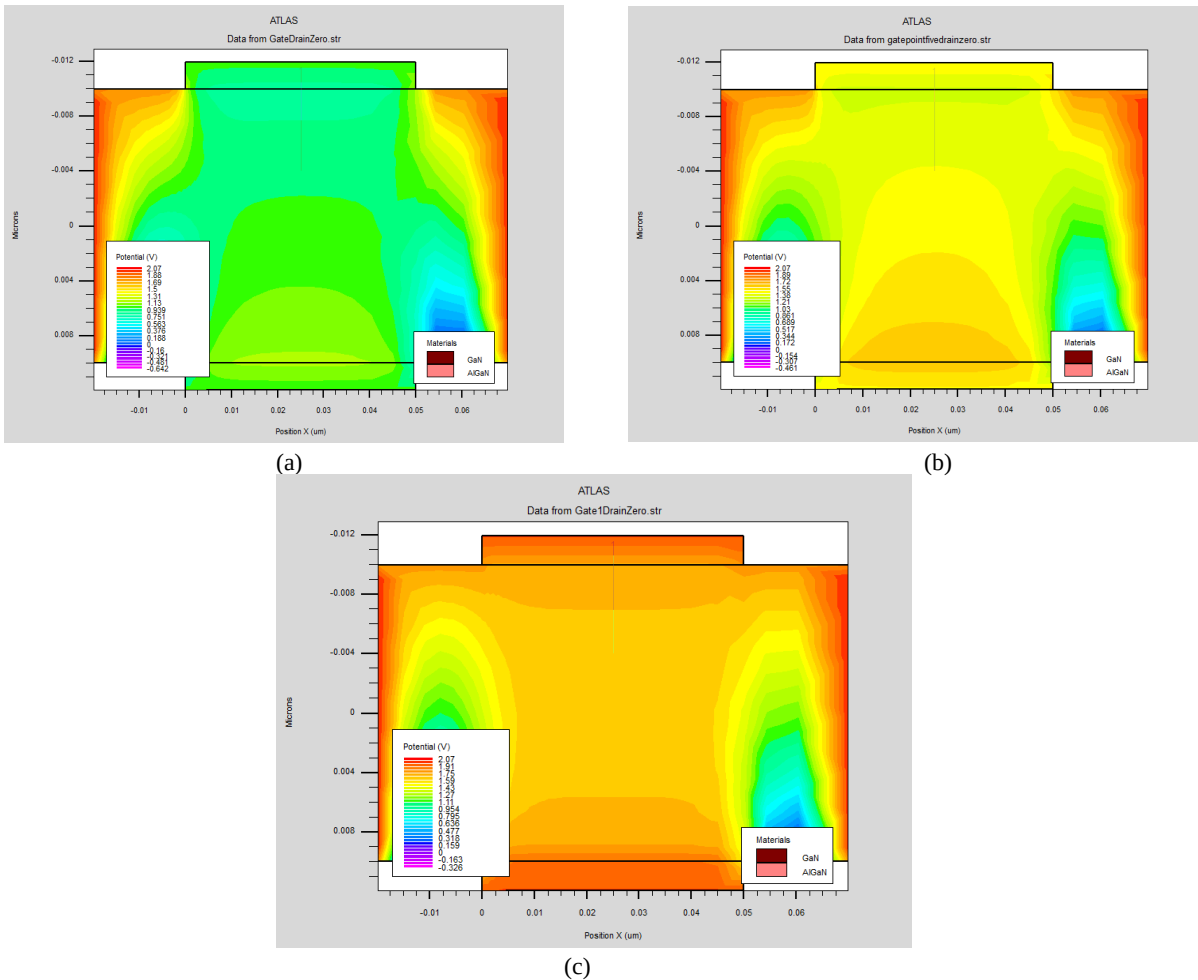


Fig. 3: Potential Contour at $V_D=0$ (a) $V_G=0$ V (b) $V_G=0.5$ V (c) $V_G=1$ V

The energy band diagram of the proposed model w.r.t. V_D and fixed ($V_G=0$ V) is represented by Fig. 4(a-b). The V_D is varied as 0.5 V and 1 V. It is evident from Fig. 4 that the effect of variation in drain voltage is less dominant in comparison to the effect of V_G .

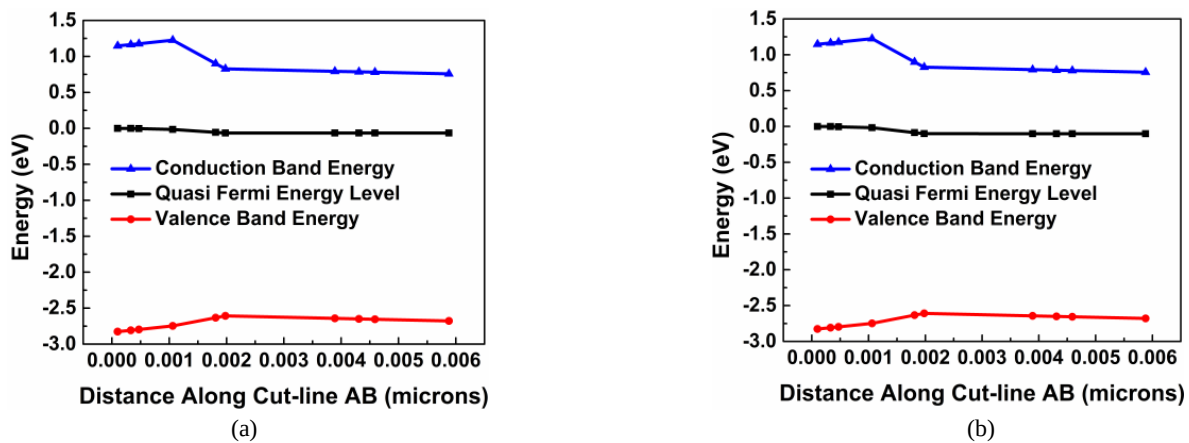


Fig. 4: Energy Band Diagram at $V_G=0$ (a) $V_D=0.5$ V (b) $V_D=1$ V

Fig. 5(a-b) represents the potential contour. The V_D is varied as 0.5 V and 1 V. The potential contour density increases with increase in V_D .

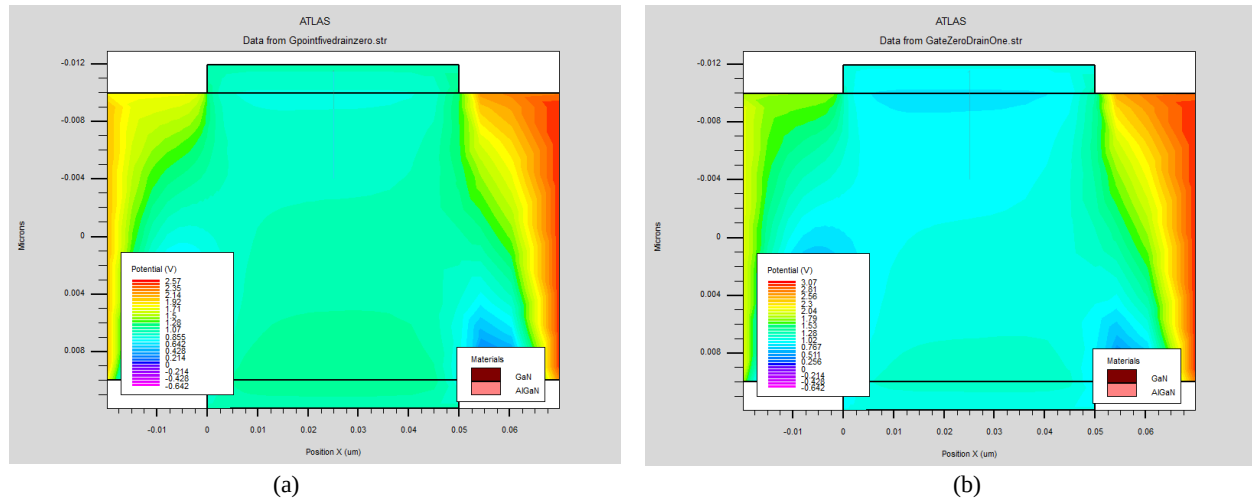


Fig. 5: Potential Contour at $V_G=0$ (a) $V_D=0.5$ V (b) $V_D=1$ V

3.1 Calculation of threshold voltage:

Fig. 6(a) and (b) represents the calculation of threshold voltage. The thickness of AlGaIn barrier layer is varied as 1, 2, 3, 4, 5, 6, 7, 8, and 9 nm. The atomic composition of Aluminium in the barrier layer is 0.30. Fig. 6(b) represents the variation of threshold voltage w.r.t. different Al composition in AlGaIn barrier layer. The Aluminium mole fraction of the AlGaIn barrier layer is varied as 0.30, 0.31, 0.32, 0.33, 0.34, and 0.35.

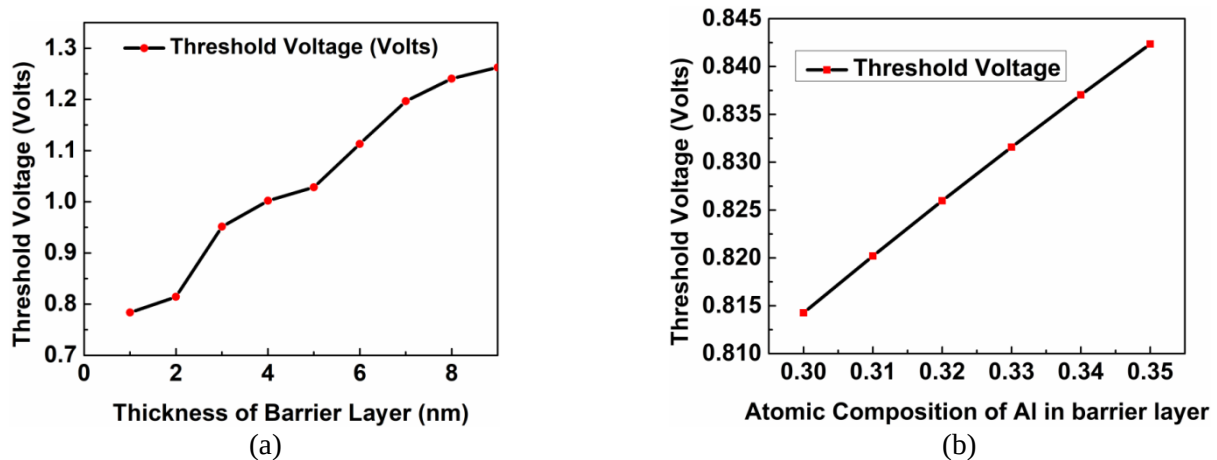


Fig. 6: Calculation of threshold voltage w.r.t. different (a) barrier layer thickness (b) Atomic composition

3.2 Calculation of drain current:

Fig. 7 represents the calculation of V_D w.r.t. V_G . The Aluminium mole fraction is varied as 0.30, 0.31, 0.32, 0.33, 0.34, and 0.35. The V_G is varied as 0, 0.5, 1, 1.5, 2, 2.5, and 3 Volts. It is evident from Fig. 7 that drain current of the devices increases with increase in mole fraction.

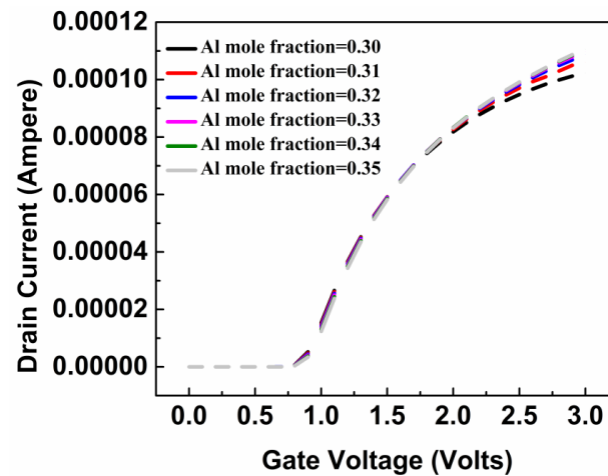


Fig. 7: Variation of Threshold Voltage with Atomic Composition of barrier layer

4. Conclusion:

A novel normally-OFF gate all around III-V FET is proposed. The threshold voltage of the device is positive, unlike previously proposed models of III-V FET. The proposed model can be used in fail-safe power switches, RF amplifiers, and in power Electronics where normally-off devices are highly desirable. The drain current of the device increases with increase in mole fraction of Al. The proposed model being normally in OFF state can be used where lower power dissipation requirement in III-V devices is on highest priority.

References:

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