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Analysis of Ingaas MOSFET For High Frequency Applications

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Abstract—A new n-channel MOSFET with $In_{0.53}Ga_{0.47}As$ as an emerging material by incorporating trench is presented. The proposed structure consists of 1 µm device width, and the gate length (L) is 40 nm with 6 nm oxide (Al_2O_3)thickness. The gate (TaN) is located in an oxide-trench built in epi-layer so the formation of channels in p-base. Gate (G) and Drain (D) contacts are placed at either side of the structure while source contact is located at the middle of the architecture. With the help of 2-D simulator the performance and characteristics are analysed, and compare the results of the proposed trench- MOS (T-MOS) with that of the planer MOS (P-MOS). The proposed T-MOS provides 1.35 times higher output current, 26% enhancement in gain (g_m), and 57% higher cut-off frequency (f_T) in comparison with the planer MOSFET.

Keywords—TaN; InGaAs; cut-off frequency; Al_2O_3.

I. INTRODUCTION

The n-channel small energy band-gap InGaAs metal-oxide-semiconductor field-effect transistor (MOSFET) becomes very popular due to abundance availability in the nature and high performance in small signal RF, and digital logic circuits. With the advantage of high electron (e^-) mobility, low energy band gap and superior injection velocity of n-channel InGaAs (i. e. III-V semiconductor) MOSFETs [1] make these transistors a suitable candidate for VLSI, Digital circuit, and high speed applications [2]. Today's researchers observed InGaAs MOSFETs as a key ingredient for future VLSI and electronics industry [3-5]. In the past two decade, Si is used as a popular material in semiconductor industry for manufacturing various e-gagets but todays the market requirement is changed. The necessity of an alternate material, the InGaAs is used as a new material. Some advancement is needed for oxide-InGaAs interface, for the development of MOSFETs with InGaAs channel. Due to the higher mobility, good oxide interface, low energy band-gap, InGaAs acts as an emerging semiconductor material is capable for obtaining high speed electronics devices in comparison to the silicon MOS devices [6-11]. For high frequency (i. e. radio-wave) applications, the semiconductor device should exhibit high drain current, maximum gain, large current ratio, low-leakage current and high gain. Although, higher the molefraction of indium in InGaAs in addition high gate-dielectrics (k)exhibit maximum output current (I) value at small drain potential with satisfactory short channel effects (i. e. SS, DIBL). InGaAs semiconductor material consists of small band-gap so it cause a leakage current in the MOS device due to BTBT phenomenon [12]. Therefore, it is very challenging task for researchers and scientist to realise improvement simultaneously in all parameters.In this research paper, we propose architecture with III-V material by introducing trench concept that can bring

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significantprogresses in the performing parameters over the planer structure. Simulations are accomplished by using semiconductor simulator (ATLAS) [13], the performance of the InGaAs trench MOSFET (T-MOS) has been reviewed andalso a comparison is accomplished with the InGaAs planer MOS (P-MOS).

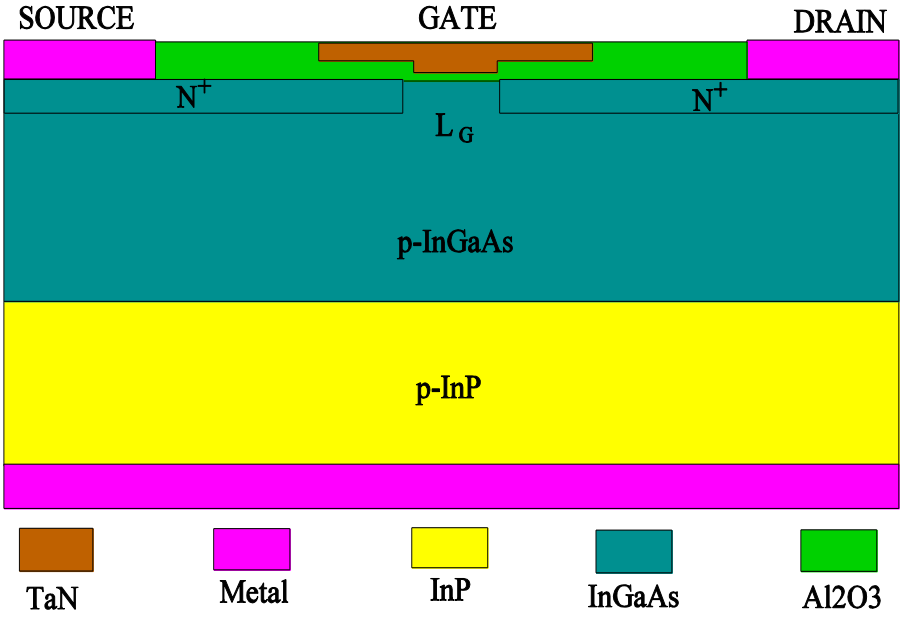

Fig. 1. Cross-sectional view of the InGaAs P-MOS

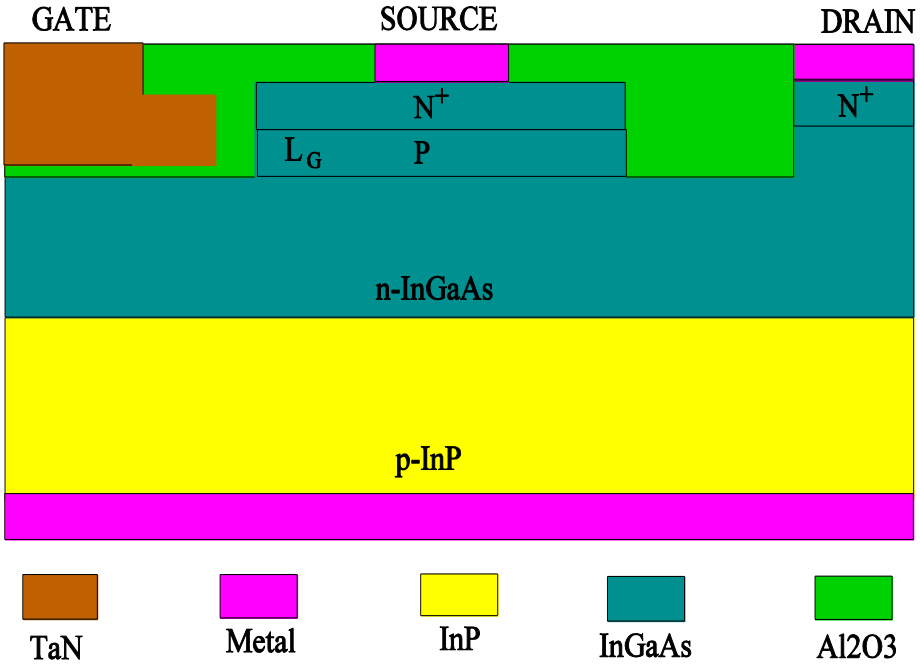

Fig. 2. Cross-sectional view of InGaAs T-MOS

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II. MOS ARCHITECTURE AND DESIGN FEATURES

The schematic view of the planer and trench-MOSFET (T-MOS) devices are shown in Fig. 1 and 2, respectively. Devices are implemented on III-V semiconductor material as $In_{0.53}Ga_{0.47}As$. In both the MOSFETs, InP is considering as substrate material. The MOSFET has a 400 nm InP layer along with 400 nm $In_{0.53}Ga_{0.47}As$ quantum well. A high concentration of $In_{0.53}Ga_{0.47}As$ cap-layer having thickness 20 nm is used for the P-MOS and T-MOS structures. The source and the drain contacts are made with the help of highly concentric InGaAs layers. The P-body is realised with doping 2×10^{18} cm^{-3} for the T-MOS and P-MOS. Devices consists of 40 nm channel length with gate-work function of 4.5 eV. In our simulations, we consider the 1×10^{12} $eV^{-1}cm^{-2}$ as an interface trap charge density. Fig. 1 depicted about the planer MOSFET which consist single source, gate, and drain contacts on the top of the structure. Only a single channel is formed in the p-base,once the gate potential value is more than the threshold potential and a current starts to flows from one terminal (Drain) to another terminal (Source) for positive drain potential. However, in T-MOS, the gate contact is located in a trench made in the epi-region, a subsequent creation of higher amount of current in the channel. Drain contact is located at the corner side of structure while sourcecontact is placed in between the gate and drain electrodes. A high value of input supply produces conducting channels in the T-MOS and a significant value of current drifts from drain to source region via the channels. Due to high conduction of currents substantial improvements in the transconductance. The peak value of g_m in the T-MOS provides the significant role to improve the cut-off frequency.

III. ANALYSIS OF THE OUTCOMES

The T-MOS and P-MOS structures were implemented with the help of ATLAS software and simulations are carried out by considering suitable models such as CONMOB (i. e. concentration-dependent mobility), CVT Lombardi, FLDMOB (i. e. field-dependent mobility), and SRH (i. e. Shockley-Read-Hall) [9]. The characteristics of the T-MOS and P-MOS structures are compared below.

A. I-V Characteristics

The output characteristics of the T-MOS and P-MOS structures at various input drive potentials are depicted in Fig. 3 and Fig. 4. From the I-V curves of the device it is noted that the current ability of the T-MOS is considerably higher than the P-MOS for all gate potentials. At V_{GS}= 1V, the value of the saturated output current of the T-MOS and P-MOS are 0.42 and 0.31 mA/μm, respectively. This result clearly indicates the output drive current (I) value of the T-MOS is 1.35 times higher in contrast to the P-MOS. To achieve a desired output current, the T-MOS will require less width as compared to P-MOS and due to this the advantage is the reduction of fabrication area. Therefore, overall the cost advantage of the T-

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MOS over the P-MOS.The current flow line in the InGaAs planer MOSFET (P-MOS) and InGaAs trench MOSFET (T-MOS) are shown in Fig. 5 and Fig. 6.

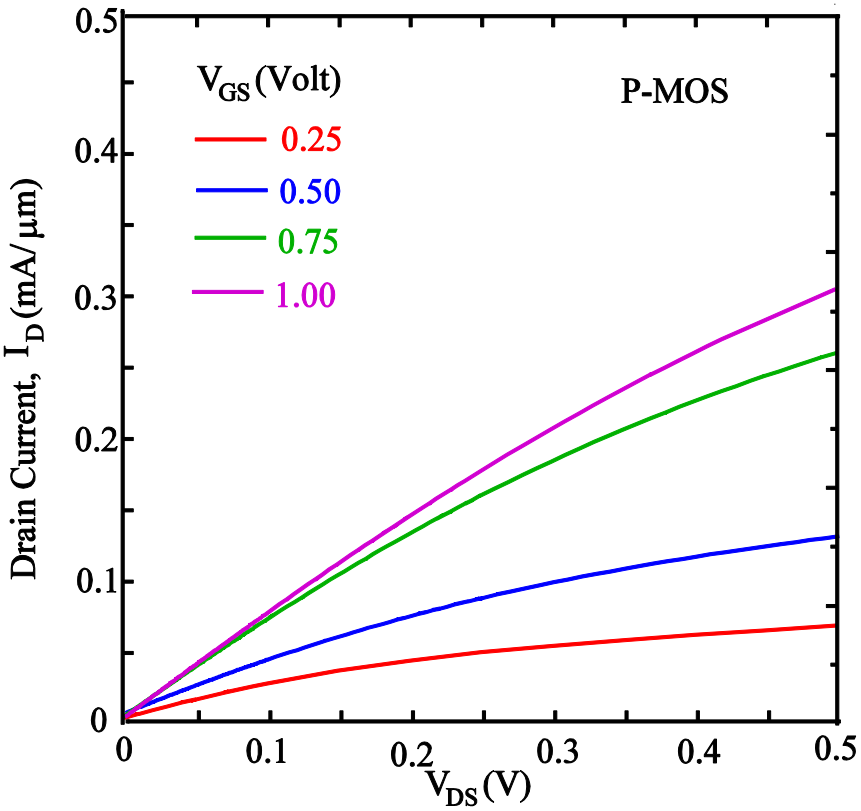

Fig. 3. I-V characteristics of the P-MOS.

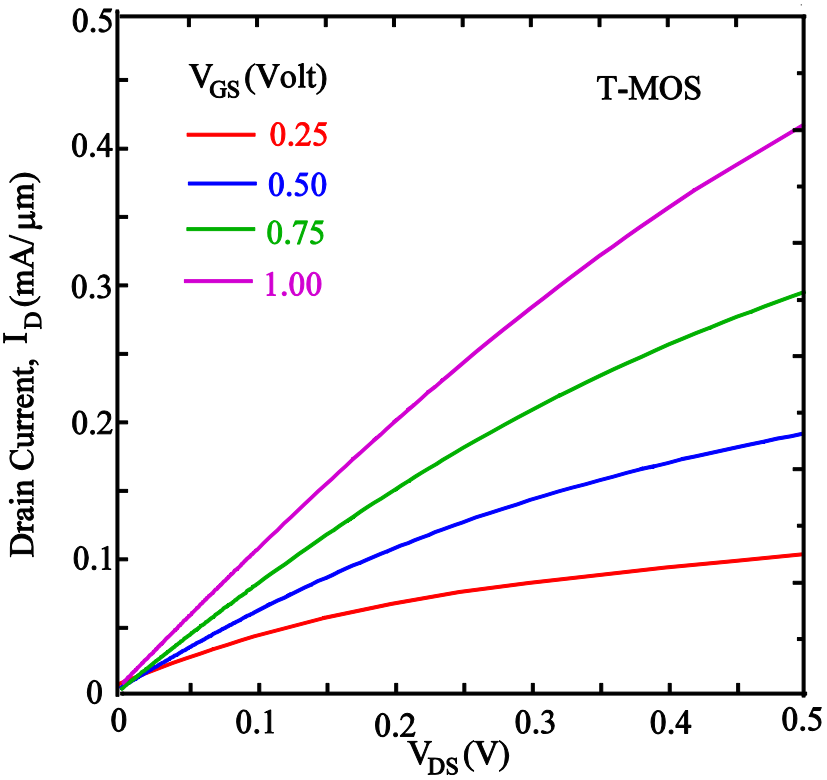

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Fig. 4.I-V characteristics of the T-MOS.

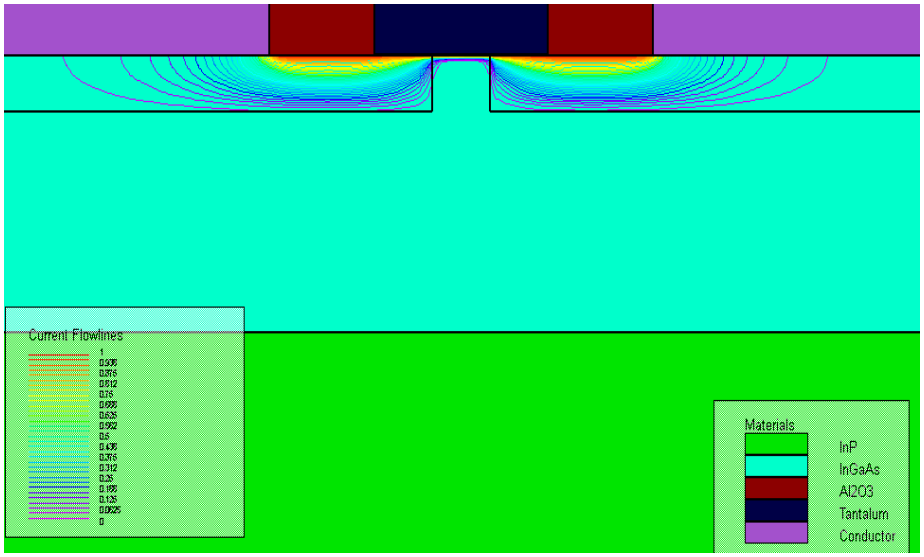

Fig. 5. Current flow line in the InGaAs planer MOSFET (P-MOS)

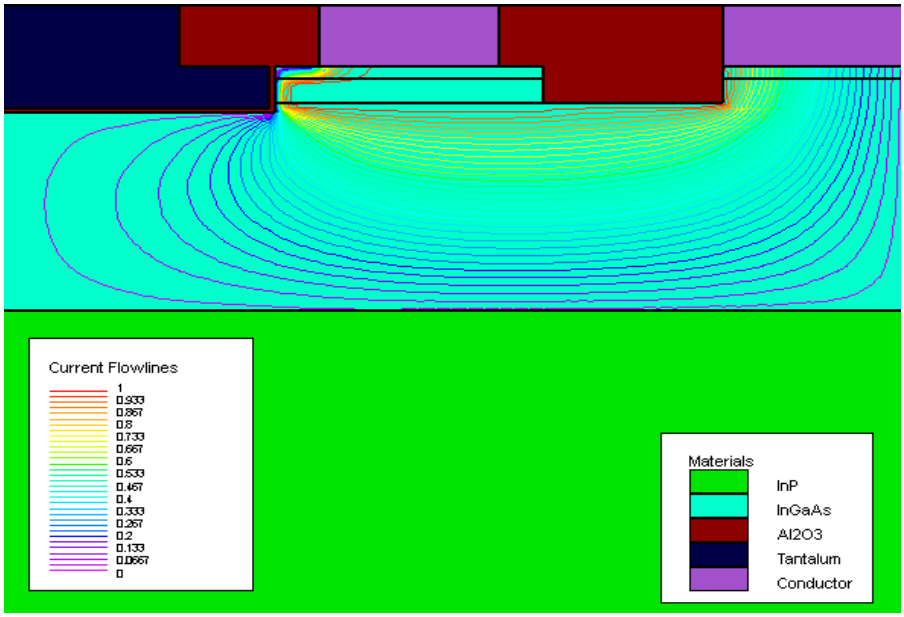

Fig. 6. Current flow line in the InGaAs trench MOSFET (T-MOS)

B. Threshold PotentialAnalysis

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The transfer curves of T-MOS and P-MOS are depicted in Fig. 7. For the extraction of threshold voltage, drawn a tangent line, at the point of the extreme slope of the curve exist on the input bias axis. The value of threshold potential in the T-MOS and P-MOS are detected 0.03 and 0.04 volt, respectively. It signifies that the T-MOS consist of lower threshold potential as compared to the P-MOS i. e. gives 33% reduction in threshold voltage.

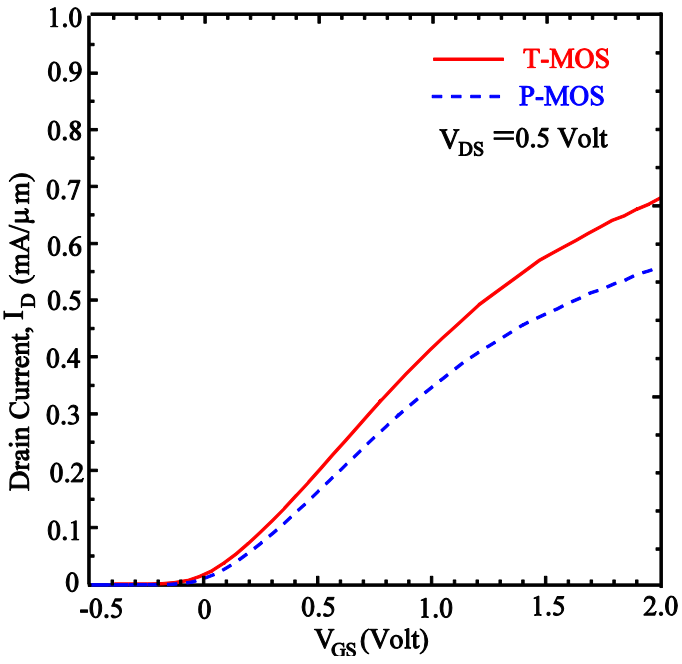

Fig. 7. Transfer curves of the T-MOS and P-MOS

C. Transconductance Curves

Fig. 8 depicted the variation of g_m or gain with input potential of the T-MOS and P-MOS. It is observed that the T-MOS demonstrates higher g_m as compared to the P-MOS. Therefore, T-MOS represents good control of gate (G) over the drive current (I). The gain (g_m) value of the T-MOS is 360 μS/μm and P-MOS is 285 μS/μm. In other words, T-MOS gives 26% enhancement in gain. This is due to the fast current conduction and structure advancement. Higher the value of transconductance makes the T-MOS a better candidate for future satellite technology and also helpful for RF applications. Fig. 9 shows the electric-field lines of the T-MOS.

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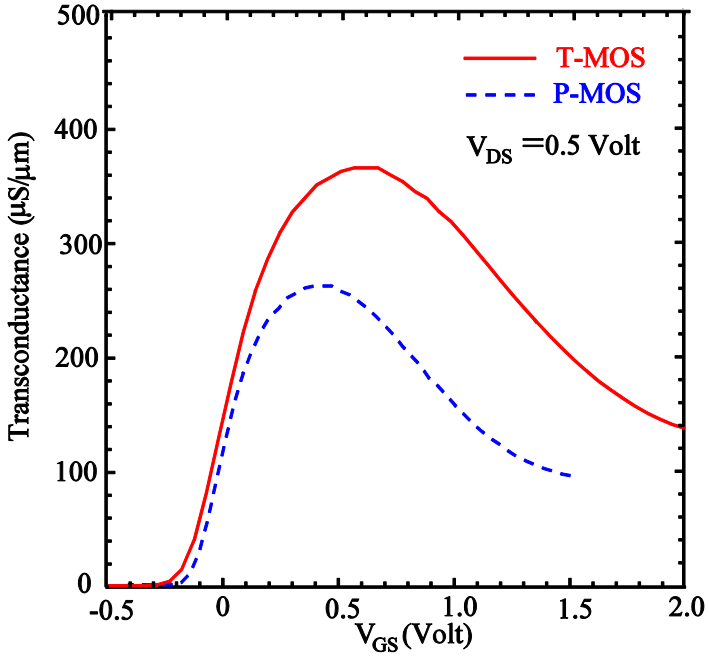

Fig. 8.Transconductance curves of the T-MOS and P-MOS

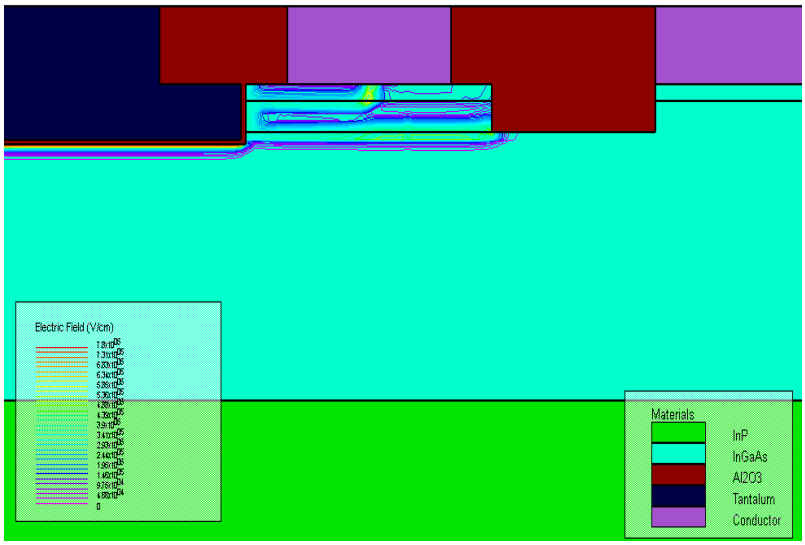

Fig. 9. Electric-field lines of the T-MOS

D. Frequency Response

The RF characteristics of T-MOS and P-MOS are depicted in Fig. 10. For the T-MOS and P-MOS device, the thickness and the gate length are 1 μm and 40 nm, respectively. In order to attain maximum value of transconductance (g_m) for both the architectures, the observed values of input bias are 0.40 and 0.65 V for P-MOS and T-MOS, respectively. The cut-off frequency (f_T) of the T-MOS and P-MOS are 25 GHz and 16 GHz, respectively. As a result, T-MOS consists of 57% higher cut-off frequency. The reason behind this is due to higher value of transconductance in T-MOS. This characteristic can be further enhanced by minimising the MOS capacitance.

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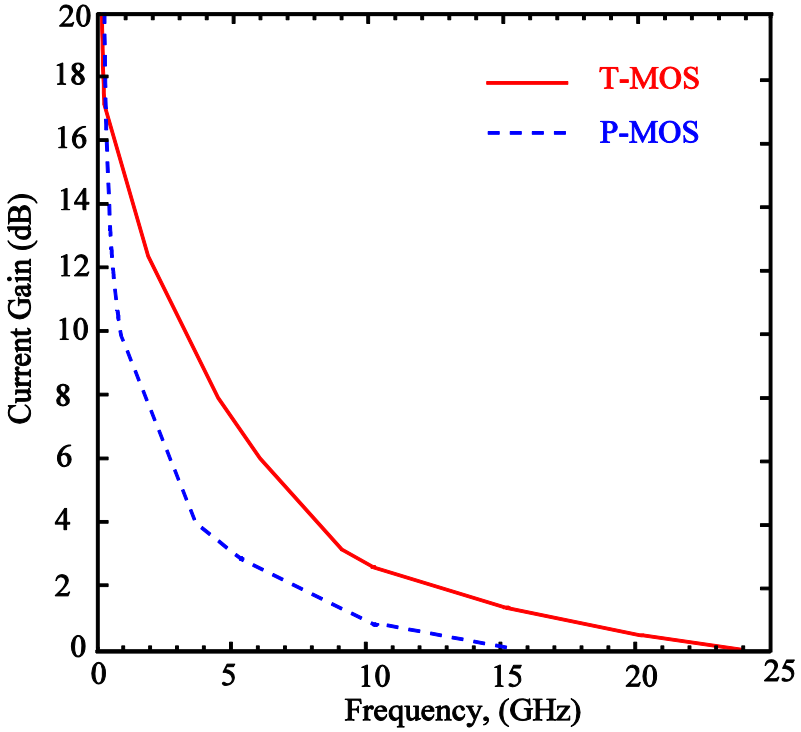

Fig. 10. Frequency characteristics(g_m) of the T-MOS and P-MOS

IV. CONCLUSION

A new $In_{0.53}Ga_{0.47}As$ n-channel MOSFET (T-MOS) with trench technology is demonstrated. The T-MOS consists of good current conduction in order to obtain the considerable enhancements in transconductance (i. e. g_m), output drive current (i. e. I_D), and cut-off frequency (i. e. f_T) for satellite and radio-frequency applications. With the help of 2D simulator analysis, the T-MOS architecture demonstrated to obtain 1.35 times higher drive current, 26% enhancement in gain (g_m), and 57% higher in cut-off frequency in comparison to the planer P-MOS. All the results indicate that substantial enhancements in semiconductor device (T-MOS) performance parameters can be achieved at the cost of some extra processing steps. The T-MOS structure is suitable candidate for future switching and low voltage applications.

REFERENCES

[1] F. Xue, A. Jiang, H. Zhao, Y.-T.Chen, Y.Wang, F. Zhou, and J. Lee, "Sub-50-nm $In_{0.53}Ga_{0.47}As$ MOSFETs with various barrier layer materials," IEEE Electron Device Lett., vol. 33, no. 1, pp. 32-34, Jan. 2012.
[2] S. Tewari, A. Biswas, and A. Mallik, "Study of InGaAs-ChannelMOSFETs for analog/mixed-signal system-on-chip applications," IEEEElectron Device Lett., vol. 33, no. 3, pp. 372-374, March 2012.
[3] J. Lin, X. Zhao, D. A. Antoniadis, and J. A. del Alamo, "A novel digital etch technique for deeply scaled III-V MOSFETs," IEEEElectron Device Lett., vol. 35, no. 4, pp. 440-442, April 2014.
[4] A. T. M. G. Sarwar, M. R. Siddiqui, M. M. Satter, and A. Haque, "On the enhancement of the drain current in indium-rich InGaAs surface-channel MOSFETs," IEEE Trans. on Electron Devices, vol. 59, no. 6, pp. 1653-1660, June 2012.
[5] M. Egard, L. Ohlsson, M. Arlelid, K.-M.Persson, B. M. Borg, F. Lenrick, R. Wallenberg, E. Lind, and L.-E.Wernersson, "High-frequency performance of self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," IEEE Electron Device Lett., vol. 33, no. 3, pp. 369-371, March 2012.
[6] S. Tewari, A. Biswas, and A. Mallik, "Impact of different barrier layers and indium content of the channel on the analog performance of InGaAs MOSFETs," IEEE Trans. on Electron Devices, vol. 60, no. 5, pp. 1584-1589, May 2013.
[7] M. S. Lundstrom, "On the mobility versus drain current relation for ananoscale MOSFET," IEEE Electron Device Lett, vol. 22, no. 6, pp. 293-295,Jun 2011.
[8] M. S. Adhikari and Y. Singh, "High Performance Dual Channel InGaAs MOSFET for Small Signal RF Applications", Electronics Letters, vol. 51, no. 15, pp. 1203-1205, July 2015.

Copyright © 2019Authors

ISSN:0971-1260
Vol-22-Issue-16-August-2019

[9] M. S.Adhikari and Yashvir Singh, "High performance multi-channel MOSFET on InGaAs for RF amplifiers",Superlattices and Microstructures, vol. 102, pp. 79-87,Jan. 2017.
[10] M. S. Adhikari and Y. Singh "Performance Enhancement of InGaAs MOSFET using Trench Technology", International Conference on Signal Processing and Communication (ICSC), March 16-18, 2015.
[11] M. S. Adhikari and Y. Singh, "Implementation of Trench-Based Power LDMOS and Small Signal MOSFET on InGaAs", IETE Technical Review, vol. 36, no. 3, pp. 1-9, Apr. 2018.
[12] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, E. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, "Impact of forming gas annealing on the performance of surface-channel $In_{0.53}Ga_{0.47}As$MOSFETs with an ALD Al_2O_3gate dielectric," IEEE Trans. on Electron Devices, vol. 59, no. 4, pp. 1084-1090, Apr. 2012.
[13] "ATLAS users manual: Device simulation software, Silvaco Int., Santa Clara, CA," 2010.

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