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# Analysis of Miller Op-Amp At 180nm Technology

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***Abstract-*** Op-amps have wide range of applications and are the basic building block in many applications. As we know that most of the signals present in environment are analog signals and when these signals are fed as input signal, the noise which is present in that signal also gets amplified. Therefore op-amp should be designed in such a way that the noise margin should be high so that reliable amplification can be achieved. This paper shows the design analysis of conventional and Miller configuration of two stage Op-amps @ 180nm technology using Cadence Virtuoso and the results of both Op-amps are concluded.

***Keywords* — PSRR, Opamp, Phase margin, Gain margin, ICMR**

## I. INTRODUCTION

Op-amps are used in many industrial and medical applications and thats why opamps are required which rejects the noise signal before amplification. Various research works are being done to achieve reliable and stable results[1-2]. Apart from stability and reliability, other parameters such as speed, power, gain, bandwidth, noise etc also plays a vital role in designing the Op-amp. Hence, designing of any Op-amp can be a challenging task.


Figure 1. Two –stage Differential amplifier

Operational amplifier plays an important role in signal systems and analog applications too. Therefore, it is essential that output of Op-amps must be stable and should be noise free. Stability of Op-amp is a major concern as if the output is not stable then the results will not be efficient and it keeps on oscillating. A desired step response is the one which reaches its final value quite early and therefore oscillations should be less which is only possible with high phase margin and therefore its phase margin should be atleast 45 degrees and practically 60 degrees. Phase margin and gain margin are the two parameters that defines the circuit's stability to a great extent. Difference of 180 degrees and the phase which is obtained at 0dB is PM.

## I. ANALYSIS OF CONVENTIONAL SINGLE-STAGE OP-AMP

Differential amplifier is the conventional op-amp. Schematic of the differential amplifier is shown in figure 1. W/L ratio of various transistors used in designing conventional single stage op-amp are compiled in table 1.

ISSN:0971-1260
Vol-22-Issue-16-August-2019

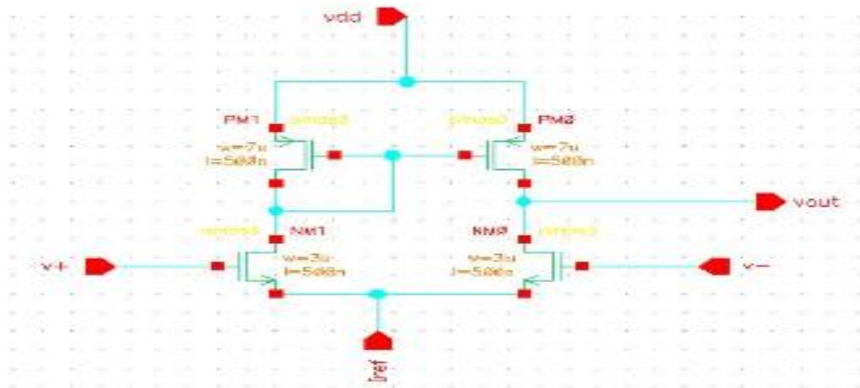


Figure 2. Schematic of Conventional single-stage op-amp

Table 1. W/L ratio of transistors of single stage op-amp

| Transistor | W/L ratio |
| --- | --- |
| PM1, PM2 | 7µm/500nm |
| NM1, NM2 | 3µm/500nm |

## II. Design Analysis of Proposed Miller two stage Op-amp

Op-amp designing mainly focuses on the various values of W/L ratio of CMOS transistors and also the capacitor value which is used for the frequency compensation purposes. These values are obtained by using different parameters like phase margin, Gain margin, ICMR, PSRR etc. In a multiple stage amplifier, the transfer function obtained using the small signal model, tells that the obtained bode plot will show two poles and one zero [5]. Design should be such that the phase margin should be atleast 60 degrees. If P2(second pole) becomes closer to GBW (GBW is the frequency after which the P2 lies) then phase margin decreases which leads to undesirable results. Now the calculation part is shown in brief to find out different values of the W/L ratio of CMOS transistors and capacitors which are used to build the design. Transfer function(Equation (i)) is obtained with the help of small signal model of Two stage op-amp. Small signal model (Figure 3) is formed to analyze the circuit and to obtain different values of capacitors used.

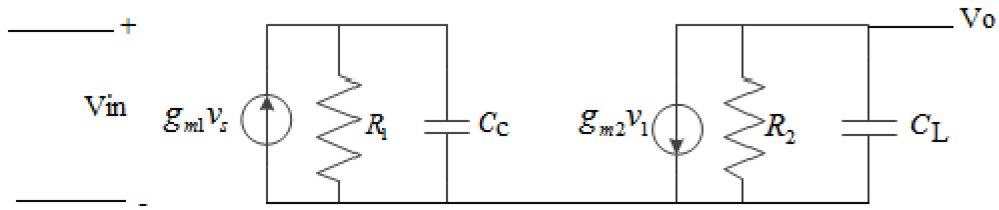


Figure 3. Hybrid model of Two-stage Differential op-amp

$$V0/Vi = \frac{(gm1.R1.gm2.R2(1-(SCC/gm2))}{[s2(R1.R2.(CC.CL)+s(R2(CC+CL)+R1(CC+CL)+CC.gm1.R1.R2]} \quad \text{(i)}$$

After solving the equation 1 different values of different parameters are obtained as shown below

$$P1 = \frac{1}{2agm1.R1.gm2.R2.CC} \quad \text{(ii)}$$

 

ISSN:0971-1260
Vol-22-Issue-16-August-2019

$P2 = \frac{gm\,2}{C2}$ (iii)

$Z = \frac{gm\,2}{CC}$ (iv)

DC Gain = gm1.R1.gm2.R2 (v)

GBW = DC gain * P1

Now putting values of DC Gain and P1 from 5 and 2 to Equation (vi) therefore, GBW becomes
GBW = gm1/CC (vi)
According to bode plot of the transfer function, dominant pole P2 will come after GBW. After putting values of poles, zero and DC gain in (i)
Vo/Vi = 4.7

Calculations
i). To calculate value of CC(Coupling capacitor): Phase margin plays important role in design specifications as discussed. Phase angle can be obtained using the equation which will be in terms of GBW.

Angle(Vo/Vi) = $-\tan^{-1}(w/z) - \tan^{-1}(w/P1) - \tan^{-1}(w/P2)$ (vii)
Now (w) is replaced by the value of GBW which is obtained in (vi) to find phase angle at GBW. Also assuming that Z(Zero) ≥ 10 GBW, therefore angle can be written as in equation (vii).

Angle(Vo/Vi) = $-\tan^{-1}(1/10) - \tan^{-1}(gm1.R1.gm2.R2) - \tan^{-1}(gm1.CL/(CC.gm2)$ (viii)
Rewriting 4.9 in terms of ADC and GBW as mentioned in equation (ix)

Angle(Vo/Vi) = $-\tan^{-1}(1/10) - \tan^{-1}(ADC) - \tan^{-1}(GBW/P2.)$ (ix)
ADC is usually of large value. Therefore, $\tan^{-1}$ of large value will be 90 degrees.

Angle (Vo/Vi)= -180+PM (x)

Equating (ix) and (x) to get the value of P2
$-180^\circ + PM = -5.71 - 90 - \tan^{-1}(GBW/P2)$
$PM = 180 - 5.71 - 90 - \tan^{-1}(GBW/P2)$
$PM = 84.29 - \tan^{-1}(GBW/P2)$. Now assuming PM to be 90, value of P2 is obtained in 4.12

P2= 2.2 x GBW
gm2/CL= 2.2 x GBW (xi)

As assumption was made earlier Z ≥ 10 GBW . So, therefore
gm2/CC =10(GBW)
Relation between CL and CC is written in (xii)
CC ≥ 2.2 x CL (xii)
CL is chosen as 2pF since this is the typically value of the input capacitance of the probes of an oscilloscope. Therefore value of CC is 4.4pF

ii).To calculate value of gm : First the design equations for this op-amp is established. The gain and GBW of the op-amp are assumed to be 60dB and 30MHz respectively as shown below.

 

ISSN:0971-1260
Vol-22-Issue-16-August-2019

Gain, ADC= gm.Rout =60dB
GBW=gm/CL=30MHz
CL=2pF,
Therefore value of gm=60µA/V. W/L ratio of CMOS transistors is compiled in Table 2 and proposed Schematic is shown in Figure 4.

Table 2. Specification of CMOS transistors of Miller Op-amp

| Transistors | W/L ratio |
|---|---|
| M1,M2 | 3µm/500nm |
| M3,M4 | 7µm/500nm |
| M5 | 2µm/180nm |
| M6 | 87µm/500nm |
| M7,M8 | 18µm/300nm |

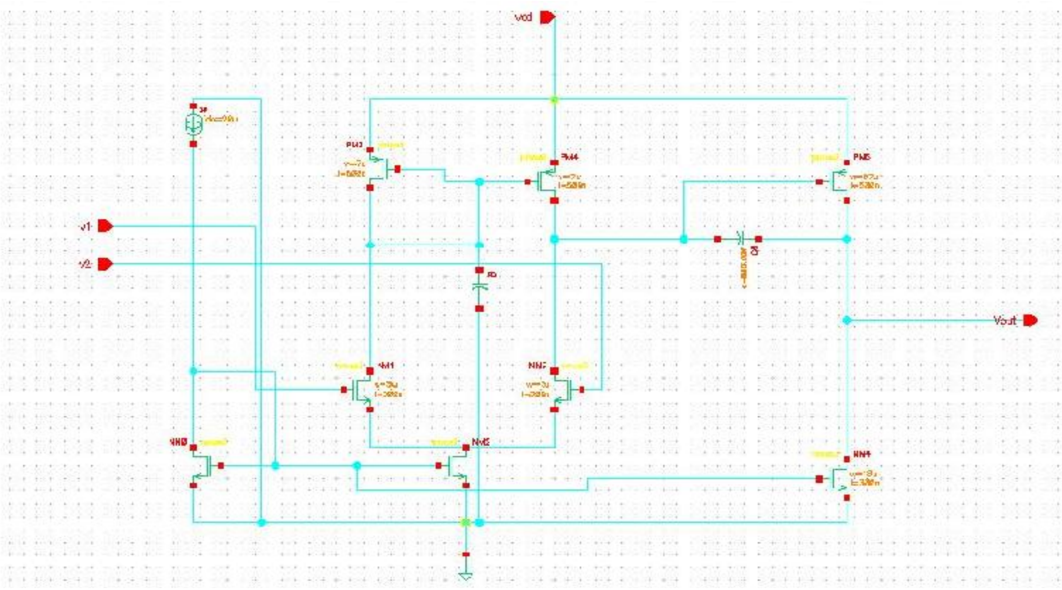


Figure 4. Schematic of multiple stage Miller op-amp

## III. Results and Discussions

As the design analysis is discussed above and accordingly the simulations were performed using cadence virtuoso at 180nm technology. The phase margin and gain margin of conventional single stage amplifier is shown in Figure 5. As it is already discussed that phase and gain margin should be high to suppress maximum

 

ISSN:0971-1260
Vol-22-Issue-16-August-2019

noise and to have stable output and therefore design of miller two stage differential amplifier is proposed. Phase margin and gain margin of the proposed design in shown in Figure 6.

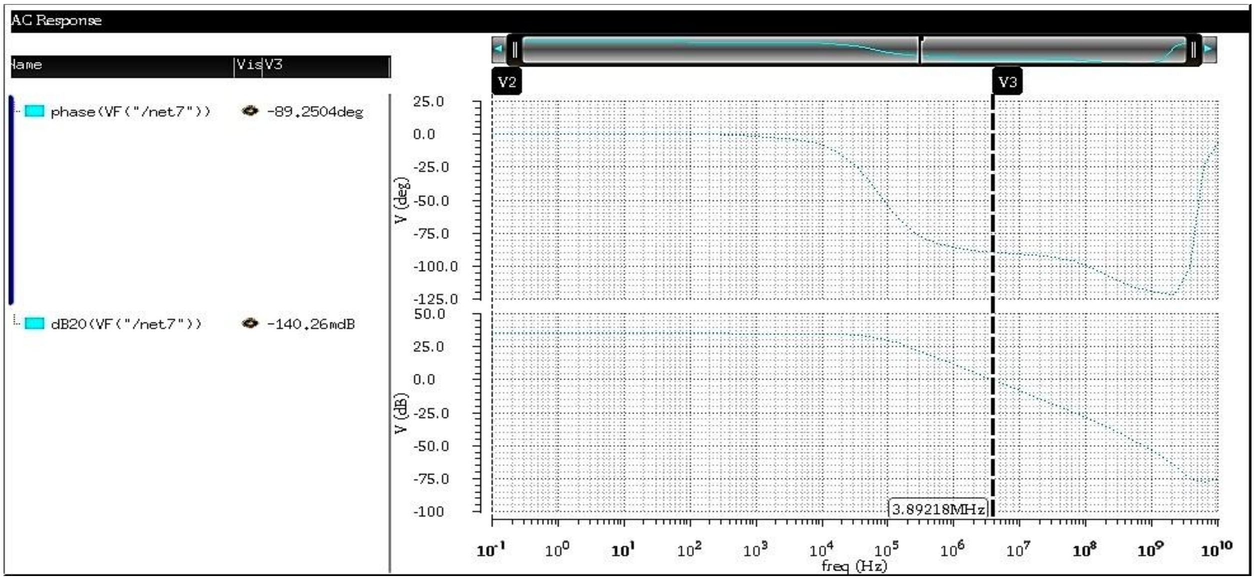


Figure 5. Phase and Gain of Conventional Op-amp

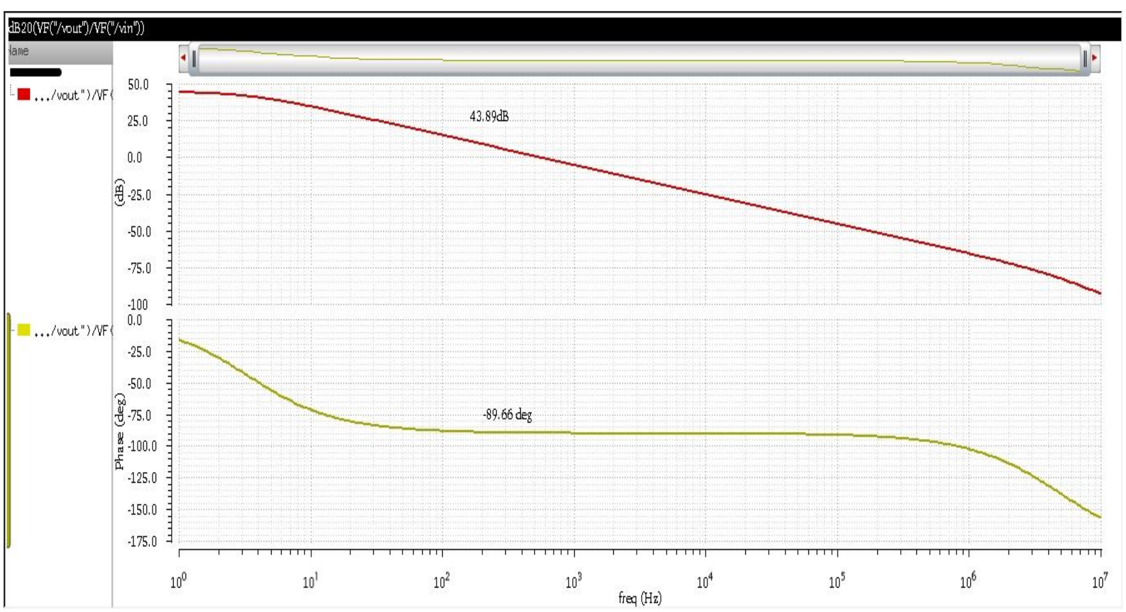


Figure 6. Phase and Gain of Miller op-amp

Table 3 Camparison of single-stage and two-stage op-amps.

| Parameters | Conventional op-amp | Miller compensated op-amp |
|---|---|---|

ISSN:0971-1260
Vol-22-Issue-16-August-2019

| | | |
|---|---|---|
| CMRR(dB) | 39 | 77 |
| Phase margin(Degrees) | 89 | 89.06 |
| Gain(dB) | 36 | 43 |

## IV. Conclusion

Keeping in notice that Opamp which are the building blocks of amplifiers which are used in ECG,EMG[8] etc should obtain a stable and noise free output. Hence, the proposed op-amp which is a TWO-STAGE SINGLE Miller op-amp has high gain and phase margin. Camparison of single and two-stage op-amps are made in Table 3. The entire design has been done in 180 nM TECHNOLOGY USING CADENCE TOOL. PROPOSED miller op-amp shows phase margin of 89degrees and gain of about 43dB. All results have been obtained using cadence virtuoso at 180nm technology.

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