THINK INDIA Journal

ISSN:0971-1260
Vol-22-Issue-16-August-2019

Design of 4-Bit Flash ADC Using Static and Dynamic TIQ Comparator

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***Abstract*—**In this work a high speed flash ADC based on threshold invert quantization (TIQ) comparator has been proposed. Unlike conventional ADC resistive ladder and comparator bank has been replaced by TIQ comparator which compares the varying input with in-built switching potential, 2^n-1 number of TIQ requires with different switching for n-bit ADC. 4-bit flash ADC has been implemented with static and dynamic TIQ; Different threshold of static TIQ is obtained by scaling the width of PMOS and NMOS individually while in dynamic TIQ input to each inverting stage acts as body voltage decide threshold voltage dynamically, threshold of TIQ is function of individual MOS width and body potential. Cadence Spectre based simulation result show that static TIQ should preferred for low power and dynamic TIQ for high speed.

Keywords—ADC; TIQ comparator; Body Bias; Encoding;

I. INTRODUCTION

Flash ADC is considered as fastest of its type, but it suffers from large number of comparator and power hungry resistors. Resistive ladder set different reference voltage statically and compared with time varying signal, an n-bit flash ADC requires 2^n-1 number of comparator followed by encoder. A variable threshold voltage comparator based flash ADC discussed in [1] using scaling and body bias effect, with high conversion time. Resolution of ADC depends on minimum voltage has been approximated for one step, to have high resolution structure increases and result in high power consumption [2]. In this work flash ADC architecture investigated based on two different TIQ comparator (a) static TIQ- vary threshold voltage using scaling width of MOS and (b) dynamic TIQ - vary threshold voltage using body biasing[2]. Structure of paper is organized as follows section 2 describe the static and dynamic TIQ. Comparative simulation result of flash ADC with static and dynamic TIQ presented in section3 finally concluded in section4.

II. TIQ COMPARATOR

A. Static TIQ comparator

Fig1 presents static threshold invert quantization (TIQ) comparator. TIQ comparator is a cascaded structure of 2 CMOS inverter. First stage of TIQ sets the threshold of comparator and second stage is gain booster. Threshold voltage of comparator is decided by resistance offered by

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ISSN:0971-1260
Vol-22-Issue-16-August-2019

PMOS and NMOS transistor. A TIQ comparator offers in built reference voltage to compare the varying input signal. Resistance ladder ADC requires resistance network of create different reference voltage result in high power requirement where 4-bit flash ADC used multiple TIQ comparators to have multiple references voltages. First inverter stage set different voltage level by changing the width, length is kept constant. Second stage of inverter increase gain and inserts the logic level [3].

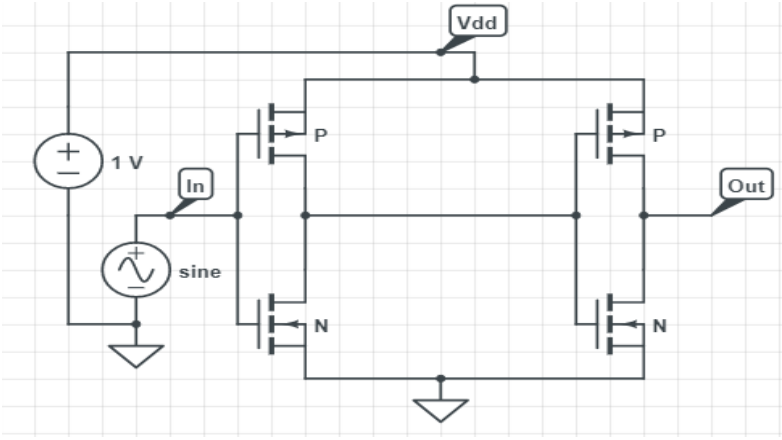
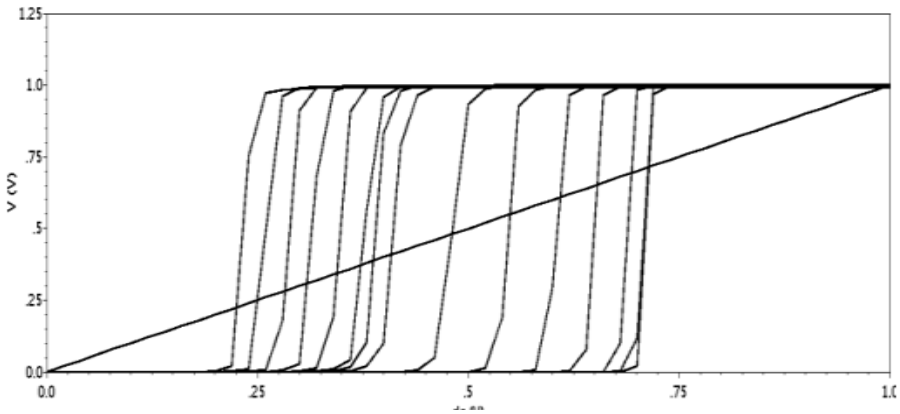


Fig1 Static TIQ comparator

TIQ comparator exploits the usage of voltage transfer characteristic (VTC) curve to determine its threshold as reference, intersection point of input and output curves set its threshold voltage calculated from equation(1).

$$Vs = \frac{(V_{dd} - |V_{tp}|)\sqrt{(K_p/K_n)} + V_{tn}}{1 + \sqrt{(K_p/K_n)}} \qquad (1)$$

Where Vtp and Vtn is the threshold of PMOS and NMOS, switching voltage of TIQ comparator strongly depends on width of MOS since Kp= µpCox (W/L)p and Kn = µnCox(W/L)n. By varying the width of each transistor different switching voltage obtained for individual TIQ. Firstly TIQ has been designed at Wp=Wn, Threshold increases by increasing Wp while Wn kept constant and threshold decreases by decreases by increases of Wn while Wp kept constant. In this work Wp ranges from 120nm to 30um, Wn is constant and Wn ranges from 120nm to 13.6m, Wp is constant. Fig 2 presents cadence spectre based parametric analysis of 16 TIQ has been performed for ramp input ranges from 0 to 1V.



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ISSN:0971-1260
Vol-22-Issue-16-August-2019

Fig2 Switching voltages of TIQs

B. Dynamic TIQ comparator

A dynamic TIQ utilizes body biasing effect in addition to decide its threshold. Input signal dynamically connected to body terminal of each MOS result in faster comparison. Threshold voltage of inverter is determined by equation(2) [4].

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right) \quad (2)$$

Where VT0 is threshold at zero substrate bias and γ is substrate bias coefficient. Threshold voltage depends on substrate bias too. Fig3 shows the dynamic TIQ; incorporates both scaling down of width and substrate bias for obtaining different switching voltage.

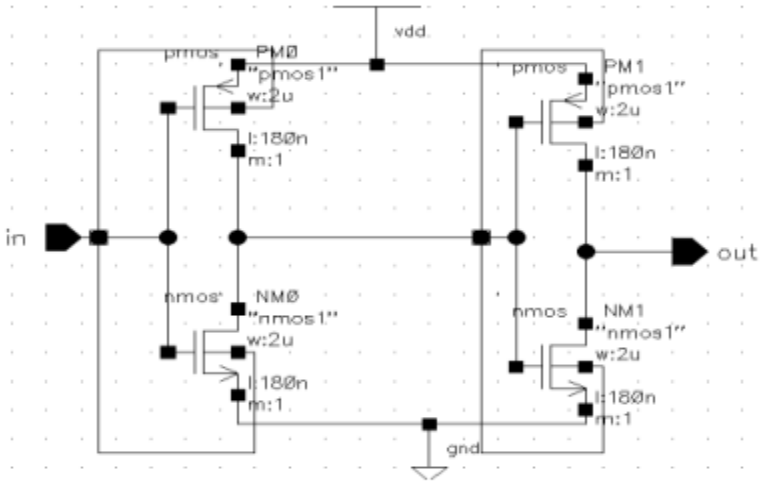

Fig3 Dynamic TIQ

A rising input increases the threshold of NMOS and decrease for PMOS, similarly falling input decrease the threshold of NMOS and increase for PMOS. Threshold voltage of TIQ is function of width of MOS devices and input signal. For dynamic TIQ Wp ranges from 120nm to 10um when Wn kept constant and Wn ranges from 120n m to 580nm, Wp is constant. A static TIQ comparator requires 87.47us to digitize the input while dynamic TIQ only takes 42.03us.

III. FLASH ADC & SIMULATION RESULT

Flash DC in [1] interface diagram of 4-bit flash ADC, ADC requires comparator bank which compares the input signal with inbuilt switching voltage and an encoding circuit. A ramp signal is applied to 15 comparator in parallel, for minimum input peak lowest comparator compares with inbuilt switching voltage and produces T1=1 and so on. Output array of comparators are known as thermometer code, multiplexer based encoding scheme developed in [5-8] has been utilized to convert in binary logic. Flash ADC [1] Cadence virtuoso schematic composer has

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ISSN:0971-1260
Vol-22-Issue-16-August-2019

been used for designing at CMOS 90nm technology and spectre for result simulation, Transient analysis of ramp signal from 0 to 1V is applied to flash ADC based on static TIQ. Digital code has been correct obtained from 0 to 15. A comparative analysis of ADC based on static and dynamic TIQ has been listed in table1. Fig4 Simulation result of static TIQ based flash ADC Fig5 Simulation result of dynamic TIQ based flash ADC

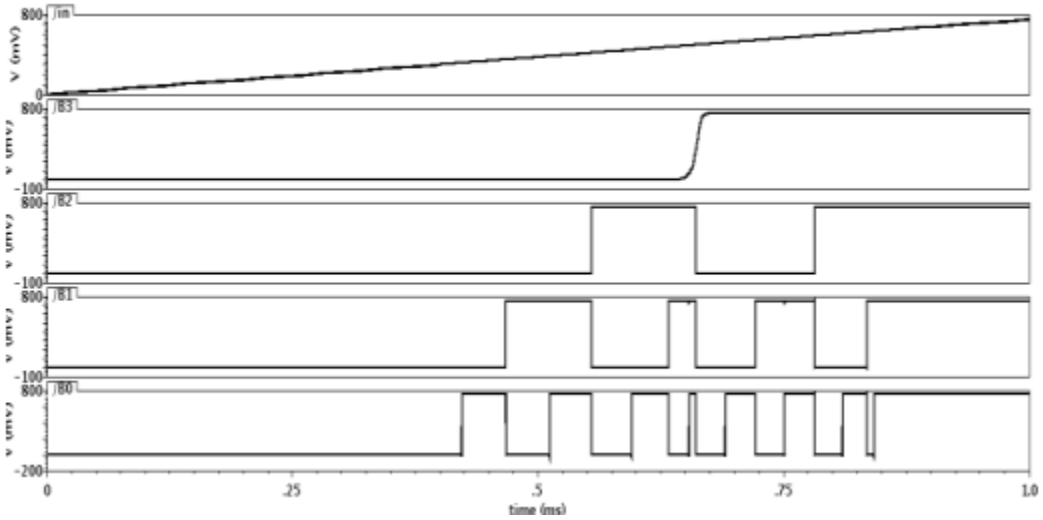

Fig4 Simulation result of static TIQ based flash ADC

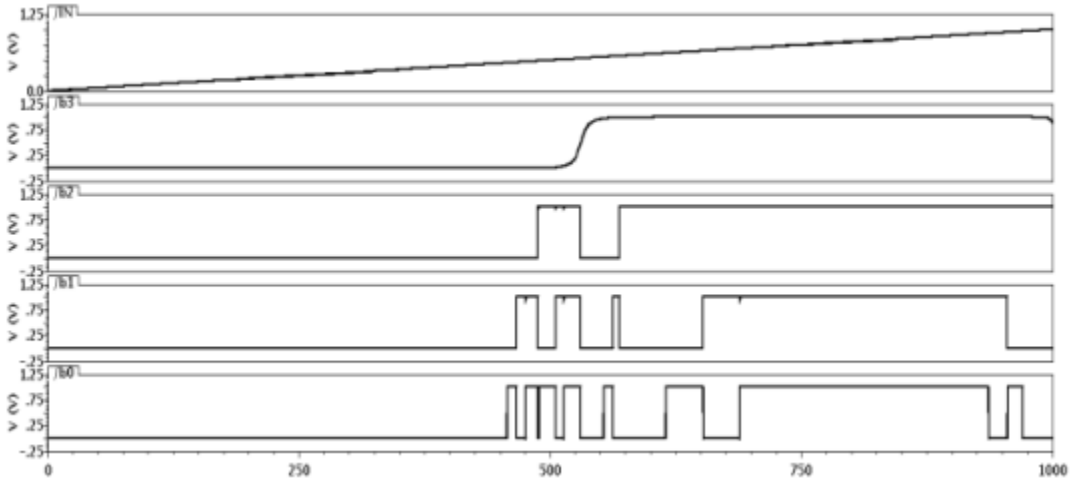

Fig5. Simulation result of dynamic TIQ based flash ADC

Table1 Comparison of static and dynamic flash ADC

	Static TIQ Flash ADC	Dynamic TIQ Flash ADC	[1]	[3]
Power (W)	30.15u	3.77m	14.08u	34.97u
Delay (s)	212.7u	40.31u	200u	230p
PDP (J)	8.6n	0.152n	2.8n	8.04n
Power Supply(v)	750m	750m	800m	1.8
Technology (nm)	90	90	90	180

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ISSN:0971-1260
Vol-22-Issue-16-August-2019

IV. CONCLUSION

The TIQ comparator is preferred due to its low power consumption but it suffers with large delay, in this work body biasing method used to enhance the comparison speed. Simulation result shows that a dynamic TIQ operates at more than double speed than dynamic but consumes high power due to more leakage. Power delay product of dynamic TIQ based flash ADC is less than 1/99th value of static TIQ based flash ADC.

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