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Comparison of Performance Analysis of 6T, 7T, 8T, 9T and 10T-SRAM Cells In Terms Of Low Power Dissipation And Delay

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Abstract: Today data storage very much important in daily life .So for this we required sophisticated electronic devices for storage purpose. So we have to design basic SRAM Cell because of SRAM has less static Power compared to DRAM. In this paper all types of SRAM cells are used like 6TSRAM, 7TSRAM, 8TSRAM, 9TSRAM, 10TSRAM cells using Dcsh and Microwind software Tools. In this connection comparing the existing &proposal design SRAM cells in term of less power dissipation and delay by the same Tools.

Keywords: 6TSRAM, 7TSRAM, 8TSRAM, 9TSRAM, 10TSRAM, Power Optimization and Delay, Dsch and Microwind.

1. Introduction

Nowadays data storage is gaining more importance in human life. All electronic and digital devices need memory for reducing the power consumption. The concept of "more data in less space" is useful for increasing the system performance and overall system efficiency. Generally we used semiconductor memory as "SRAM". SRAM can be abbreviated "Static Random Access Memory". Many VLSI chip can have SRAM memory because of their large storage capacity and fast accessing time. Where, the word static indicates that it does not need to be habitually refreshed but the DRAM need habitually refreshed. DRAM can be abbreviated as "Dynamic Random Access Memory" which is another type of memory. Both the memories can be classified from "Random Access Memory: (RAM). In this paper the power analysis of 6 transistors SRAM is compared with 7 transistor SRAM. As a result the power dissipation of 7 transistors is high when compared with 6 transistors. The power dissipation of 6T SRAM is about 2.991mW and the power dissipation of 7T SRAM is about 3.183Mw.SRAM are mostly used for mobile applications, because of their ease of use and low leakage of power. In this paper the schematic of 6T SRAM,7T SRAM, 8TSRAM, 9TSRAM and 10TSRAM, are drawn using DSCH software and the layouts are drawn using MICROWIND software

Until recently, silicon based field effect transistors (FETs) considered as ubiquitous device material for semiconductor industries. However as the transistor size gets scaled down to nanometer regime, silicon based transistors possess lots of problems like high power consumption in idle state due to large leakage, gate losing control of channel, difficulty in choosing suitable oxide material, inability to shrink oxide thickness accordingly, and various other short channel effects (SCEs). Particularly, below 10 nm, complementary metal oxide semiconductor (CMOS) has hit the power wall, that is,nonscaling of KT/q and hence no scalability of Vth and VDD.Furthermore, at those technology nodes, crystalline silicon breaks down into amorphous silicon making them infeasible to be used as a suitable material for future electronics. Thus to make future electronic devices smaller, smarter, and computationally efficient, it has become very important to opt for alternative device materials or alternative device concepts. As a result, various alternate building materials like FinFETs, grapheme FET (GFET) [1–3], grapheme nanoribbon FET (GNRFET), carbon nanotube (CNT) [4, 5], and Si-nanowire FET have been extensively studied as a future replacement for CMOS technology. Carbon nanotube has been considered in this paper due to its

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Vol-22- Issue-14-December-2019

extremely low feature size (around2 nm), high performance in terms of speed, and power consumption.

In recent days, Static Random Access Memory has become the major part in digital world. Because which occupies the largest portion of SOC (system-on-chip). The device need SRAM memory mainly for device dissipate small amount of power. But the dynamic power dissipation causes problems in digital circuits because the dynamic power depends on supply voltage, switching frequency and output voltage swing. Dynamic power dissipation can be minimized by reducing the supply voltage. At the same time low supply voltage leads to performance degradation and also decreases the threshold voltage which in turn increases the sub threshold current hence the static power dissipation increases. This paper discuss about the power dissipation of 6 transistors and 7 transistors SRAM. It also includes the functional view of 6T and 7T SRAM cells.

2. Related Work:

Many researchers have suggested a numbers of the techniques for SRAM cell design. A brief evaluation of a few significant Static RAM cell designs is existing in this part.

Byung-Do Yang [5] proposed a small power Static RAM using BL accuse recycle for understand writing and put in writing operations. This proposed charge recycling SRAM design was based on the hierarchical BL architecture and BL charge recycling method. The proposed method was achieved less degradation of SNM, 17% & 84% of read and write power consumption respectively achieved. other than the operation speed is inadequate to 145MHz

W. Kang *et al.* [9] introduced a non-volatile SRAM propose with Magnetic Tunnel Junction. They designed MAP of the MTJ device. The switching techniques provided better accumulate power, delay, and dependability disquiet. The main limitation of the system is, it consumes more switching power.

A. Makosiej *et al.* [10] introduced TFET-based 8T SRAM cell. The 8T SRAM cell maintains full functionality in all operation modes at 1V supply voltage with no architectural limitation linked to the half-selection problem. The cell design allowed the use of long word lines with bit interleaving. The major drawback of the Static-RAM design is, whenever the supply voltage increases, at the time substantial leakage power also increases.

E. Karl *et al.* [11] proposed a huge presentation, voltage scaling of 162 Mb Static RAM range was urbanized in 22nanometer tri-gate bulkiness equipment. The 22 nm tri-gate technology delivered a 0.092m High-Density Cell (H-DC) bit cell and 0.108 m Low Voltage Cell (LVC)bit cell. The main limitation of the very high. 6T Static-RAM design is, internal sensing delay is

These all related works have several issues like more delay and power consumption, high critical cell design. Here, the 6T-SRAM-AAM cell design is implemented to overcome these problems and to minimize dissipation of power and delay comparison of existing SRAM cells design

3. Operation of 6T SRAM cell:

When WL=0, there is no Read/Write operation in the 6T SRAM, and When WL=1 the two access transistors activated ,so immediately Rd/Wr operation will begins.

A conventional 6T SRAM consists 6 transistors which form two cross coupled inverters. This bit cell can be read and write single bit data. When a bit is stored in memory the 6T SRAM behave like a latch. The cross coupled inverter pattern which causes large area consumption which is a drawback of 6T SRAM when compared to resistive load. Conventional SRAM with 6 transistors is shown in figure 1 and 6T SRAM have three states they are read, write and hold states

3.1 Hold State

When write operation (WL=0) the accessible transistor M1 and M2 disconnect the cell from bit lines. The leakage current can be drawn from vdd.

3.2. Read State

The accessible transistor M3 and M6 should be ON when pre-charging bit and bit bar line to high.

3.3 Write state

ISSN:0971-1260
Vol-22- Issue-14-December-2019

When the WL=0, the value to be written to the bit and bit bar line. Hence we write a data value is "0", we take bit value is "0" and bit bar value is "1".and the data value is "1", we take bit value should be "1"and the bit bar value is "0"

4. Operation of 7TSRAM cell:

As like 6T SRAM, the 7T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 7T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

4.1 Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

4.2 Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.

5. Operation of 8TSRAM cell:

As like 6T SRAM, the 8T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 8T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

5.1 Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line

bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

5.2 Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.

6. Operation of 9TSRAM cell:

As like 6T SRAM, the 9T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 9T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

6.1 Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

6.2 Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.

7. Operation of 10TSRAM cell:

ISSN:0971-1260
Vol-22- Issue-14-December-2019

As like 6T SRAM, the 10T SRAM circuit also consists of two CMOS cross coupled to each other. In this circuit we additionally connect NMOS transistor to write line. And it also have two pass NMOS transistor connected to the bit and bit bar line. The access transistor N3 and N4 which are correspondingly connected to the write and read line to perform the write and read operation. Before write operation the 10T SRAM cell depends upon feedback connection. These feedback connection and disconnection can be performed by N5 transistor.

7.1 Write Operation

The write operation can be start by turning off the N5 transistor to this cut off feedback connection. When N3 is on and N4 is off the bit line bar carries complement of input data. The N5 is turned on and WL is turned off for reconnect the feedback connection to store new data. The bit line bar is discharged to "0" for storing "1" in the cell. And there is no need to discharge bit line for storing "0" in the cell.

7.2 Read Operation

When performing the read operation both read and word lines are turned to on and also the transistor N5 is kept on.

8. RESULTS AND DISCUSSIONS:

Here we analysis and discuss about the 6T SRAM, 7T SRAM, 8TSARAM, 9TSRAM and 10TSRAM cell during read and write operation. And the schematic diagram, layout and Power and delay analysis of above SRAM cells are designed and implemented by using **DSCH** and **MICROWIND** software Tools. They are given below figures respectively.

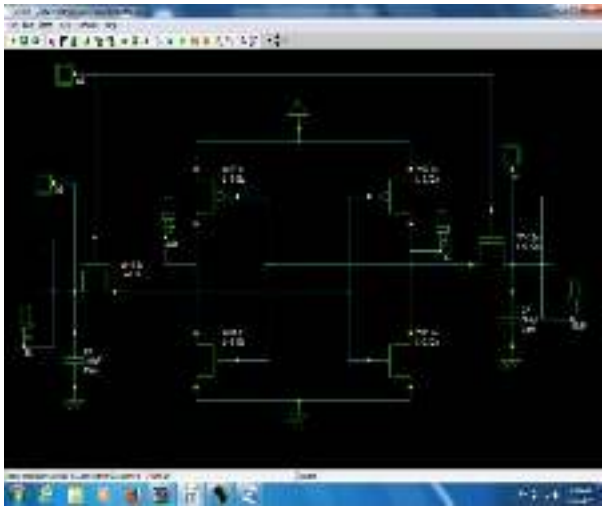

Figure.1: 6TSRAM Schematic diagram

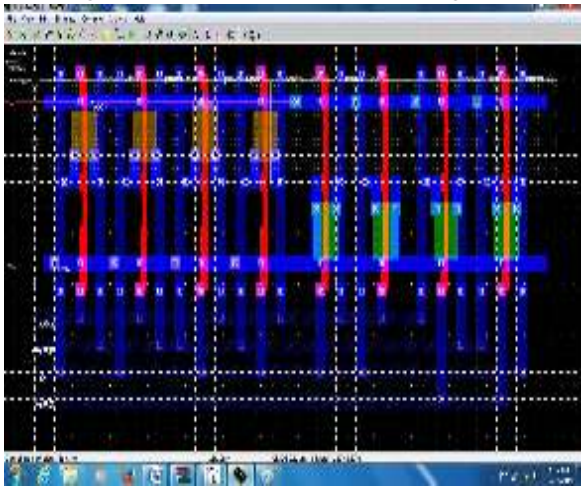

Figure.2: 6TSRAM Layout

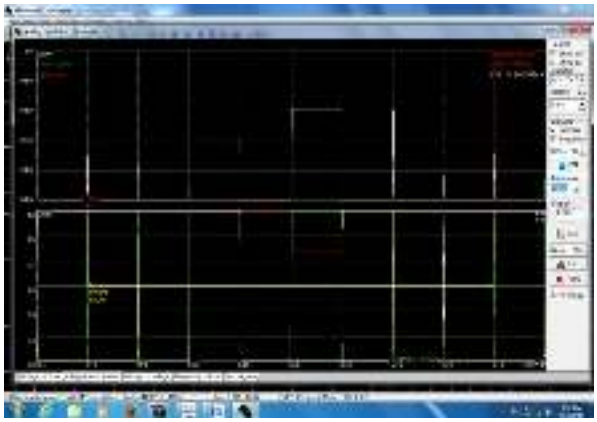

Figure.3: 6TSRAM Power and delay analysis:

ISSN:0971-1260
Vol-22- Issue-14-December-2019

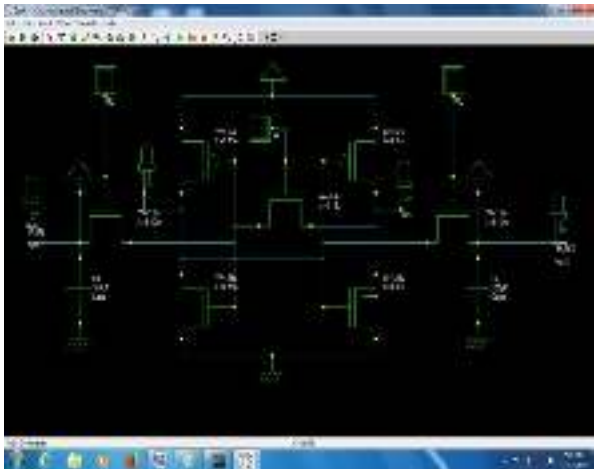

Figure.4: 7TSRAM Schematic diagram:

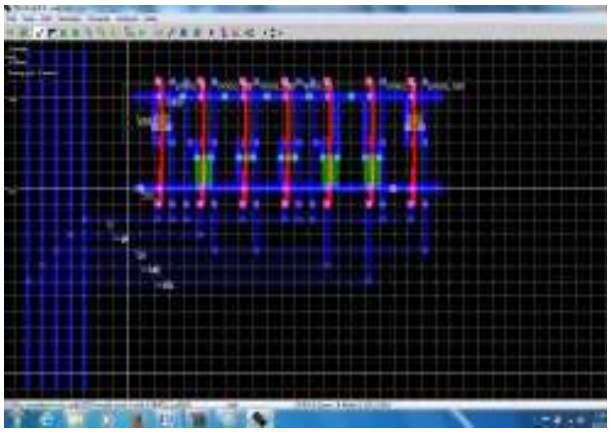

Figure.5: 7TSRAM Layout:

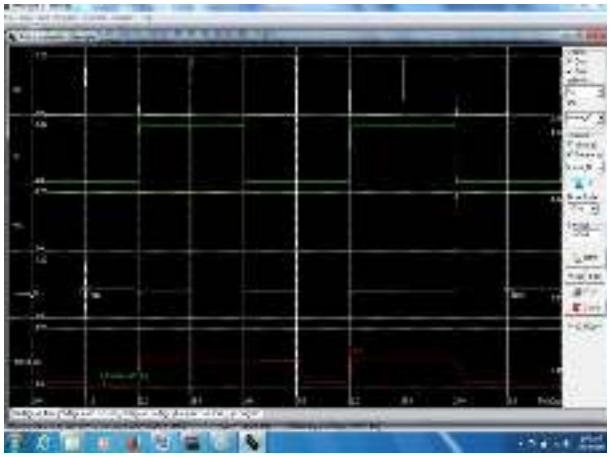

Figure.6:7TSRAM Power and delay Analysis

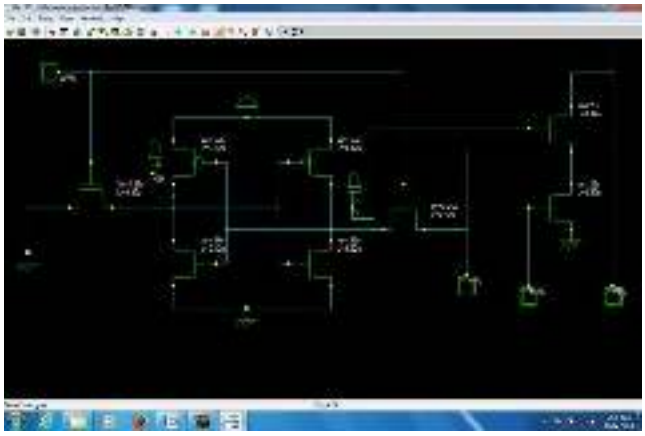

Figure.7: 8TSRAM Schematic diagram

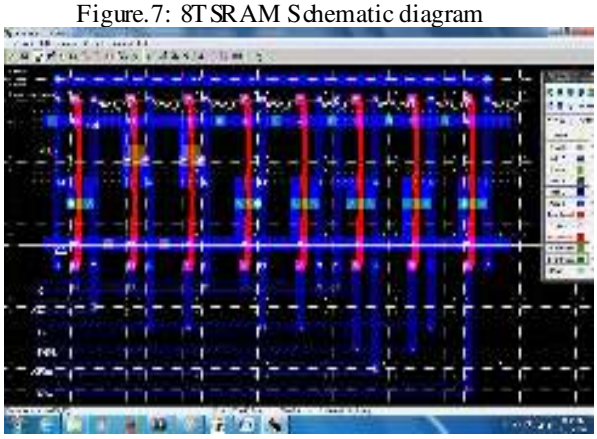

Figure.8: 8TSRAM Layout:

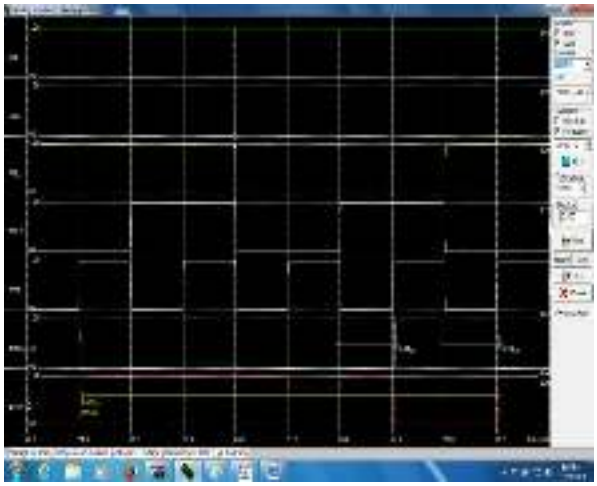

Figure.9: 8TSRAM Power and delay Analysis

ISSN:0971-1260
Vol-22- Issue-14-December-2019

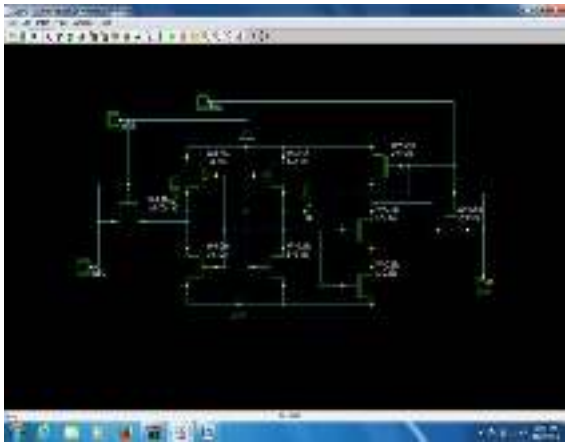

Figure.10:9TSRAM Schematic diagram:

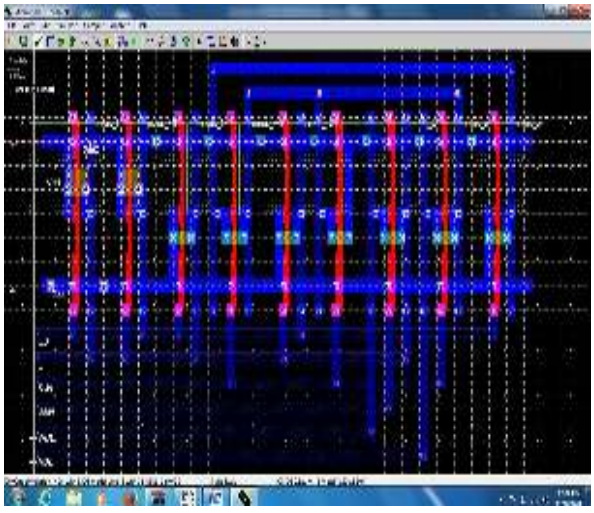

Figure.11: 9TSRAM Layout

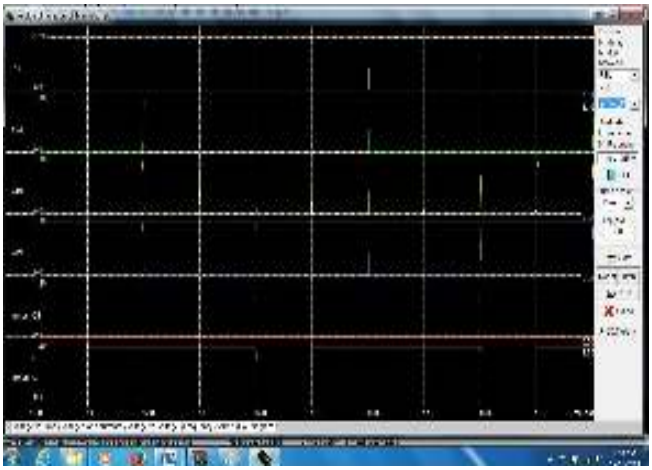

Figure.12: 9TSRAM Powers and delay Analysis

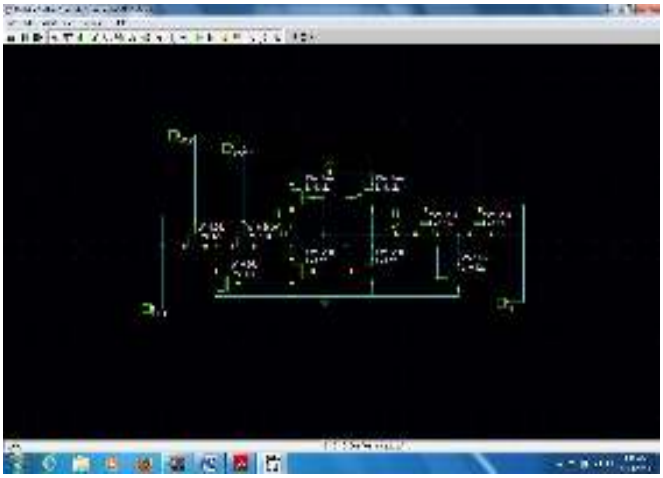

Figure.13.10TSRAM Schematic diagram

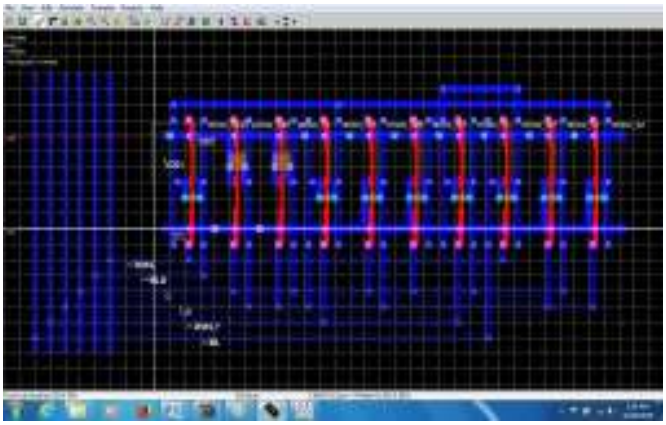

Figure.14: 10TSRAM Layout

ISSN:0971-1260
Vol-22- Issue-14-December-2019

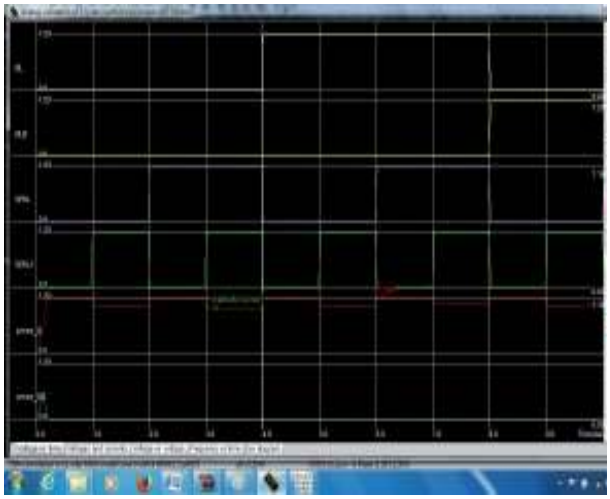

Figure.15:10TSRAM Power and Delay Analysis

Table.1: The following table shows the comparison at T=10ns period among 6T, 7T, 8T, 9T and 10T-SRAM Cells.

S. No	Type of SRAM	Static Power Dissipation	Power Dissipation (write operation)	Power Dissipation (Read operation)	Rise Time Delay	Fall Time Delay
1	6T	75.573µw	35.545 µw	75.676µw	19ps	23ps
2	7T	50µw	40.677 µw	50 µw	50ps	56ps
3	8T	18.426µw	19.130 µw	33.909 µw	3041Ps	1052Ps
4	9T	82.52µw	90.986 µw	84.426 µw	1050ps	1056ps
5	10T	54.562µw	50.242 µw	50.246 µw	1052ps	1060ps

	Rise time delay	Fall Time delay
6T	19ps	23ps
7T 8T	50ps 3041Ps	56ps 1052Ps
9T	1050ps	1056ps
10T	1052ps	1060ps

9. CONCLUSION

Finally the conclusion is that the 6TSRAM is compared among 7TSRAM, 8TSRAM, 9TSRAM and 10TSRAM cells in three factors like Area, Power dissipation and Delay paper power dissipation of 6T SRAM is compared with all above SRAM cells .It is observered 6TSRAM cell have less delay, less area and Somewhat power dissipation is high rather than all other SRAM cells. 7TSRAM, 8TSRAM, 9TSRAM and 10TSRAM cells Schematic diagram, Simulation of Power and delay analysis SRAM is desired. Simulation result shows clearly how read and write operation is performed. It is observed that the power dissipation is less as compared with ,7T SRAM to 8TSRAM, 9TSRAM and 10TSRAM . In future, power dissipation will play a major role to reduced power consumption

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ISSN:0971-1260
Vol-22- Issue-14-December-2019

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