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Pipeline ADC Using Bit Flash ADC in CMOS 90nm Technology

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Abstract— **Sampling is methodology to convert analog signal to digital. Sampling based analog to digital conversion (ADC) technique are ooversampled ADCs and nyquist-rate ADCs. Oversampling ADCs yield high resolution with the help of coarse quantizes and support input signal with low bandwidths and nyquist-rate. ADC is a better choice forsampling rate is greater than 100 Mbps. A pipelined ADC contains a large number of pipelined stage, in this workdesigned technique of each pipelined stage has been described using CMOS90nm technology.**

Keywords— Analog-to-Digital converter (ADC), flash ADC, pipeline, Sample and Hold (S&H), Multiplexer (MUX), Comparator, Encoder

1. INTRODUCTION

All of the natural signals are in analogue form. Processing of these analogue signals and converting them to digital signals is the major operation in many of the applications, which is performed using Analog-to-Digital converter (ADC) [1,2]. Analog-to-Digital converters are the major building block in many applications like Digital signal processing, communication systems, wireless systems, microprocessors and many more.Several ADC architectures had been introduced which are used to perform and attain different requirements in different applications like flash ADC, successive approximation register based SAR-ADC, delta-encoded ADC e.t.c. Out of all the ADC architectures, pipeline ADC offers high balance between conversion accuracy and conversion speed with low complexity and power consumption. A pipelined ADC consists of a number of identicalstages shown in figure1[3-5]. Input stage requires asample-hold circuit and DAC with residue calculation. The ADC output is fed into digital to analog converter (DAC) produces the analog value of corresponding to the digital input. Residueis calculatedby comparing sampled input and precede analog signal, the difference between the sampled input signal and the DAC output amplifies [6].Fig1 shows 6 pipelined stages produces 3-bits as output; therefore, total of 18-bits will be produced as outputs from all stages. These 18-bits outputs are feed in to the digital error correction block, which in turn produces 12-bit digital data as final output. Structure of paper is organized as, section2 explains internal architecture of ADC. Pipelined ADC is describing in section3 and concluded in section4.

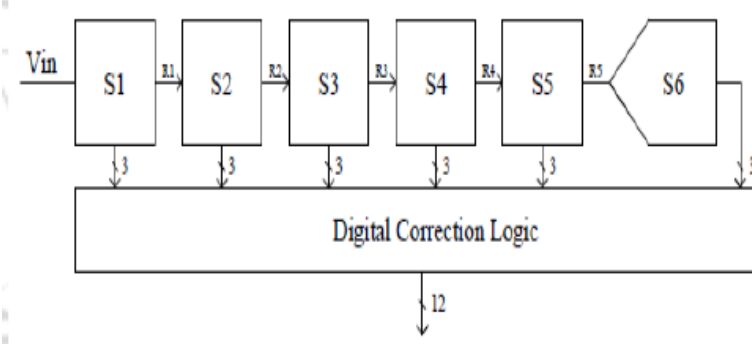

Fig. 1 12-Bit pipeline ADC block diagram

2. SINGLE STAGE PIPELINE ADC ARCHITECTURE

Each stage consists of common building blocks like sample and holds circuit, 3 Bit flash ADC, DAC, mixer and gain amplifier. Flash ADC converts the input signal into three bits and they are reconstructed back into analogue form [7-10]. Then this reconstructed signal is subtracted from the input sampled signal and the difference is multiplied by the amplification factor. Finally, we

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get a residue signal which is applied to the next stage to process.

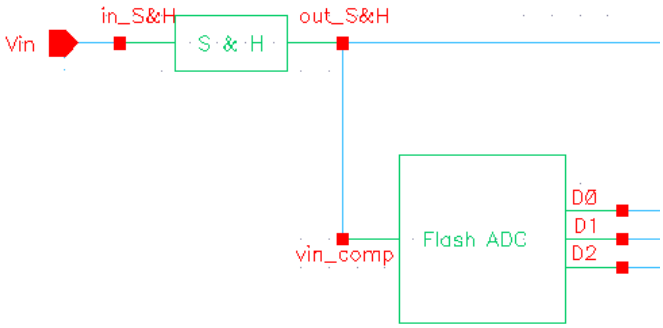

Fig. 2 1st stage of Pipeline ADC

2.1 Sample-hold circuit

A sample-hold circuit comprises of capacitor and a switch working at high sampling frequency. Switch used here is a transmission gate and hold capacitor is of 10pF. Limit of sampling frequency depends on the switch we use. In this work transmission gate acts as switch operates at higher sampling frequency.Fig3 presents the schematic of sample-hold circuit and fig4 represent sample waveform at frequency of 200MHz[11].

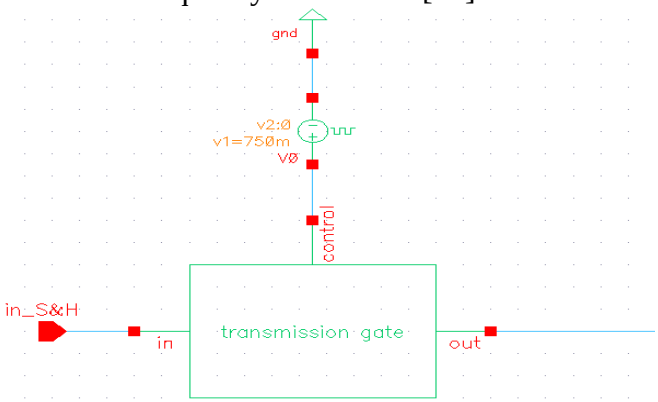

Fig. 3 Sample and Hold circuit [3,4]

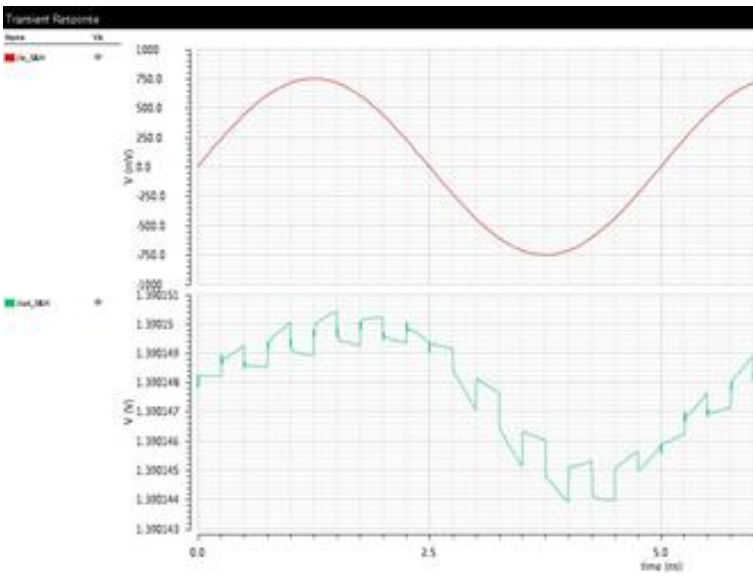

Fig 4. Sample and hold circuit transient response

2.2 Comparator

The output of comparator circuit is either logic high or logic low, which is dependent on the input and reference signals (resistive network distributed voltage). If reference signal is higher than the sampled input logic low is the output else, we get a logic high value.Therefore, for 3-bit flash ADC we require 7 comparators and 8 resistors of 1kΩ each. Each comparator produces single bit as output, output is 7 bits; consecutive 1's and consecutive 0's, these outputs are known as thermometric codes. The comparator circuit and the transient output are shown in fig. 5 and fig. 6 respectively[12]

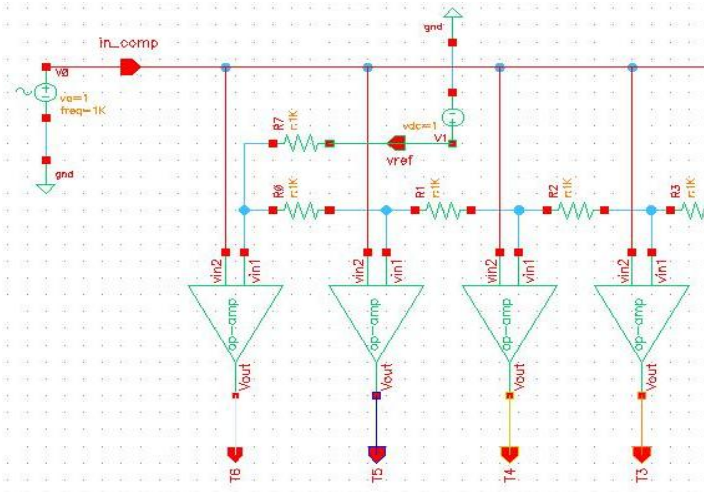

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Fig. 5 Comparator circuit

2.2 Encoder

The thermometric codes produced using comparator needs to be converted into binary codes. 2:1 mux based encoder used to convert thermometer code to binary[13]. Fig8 represents an interfaced circuit of comparator and encoder.

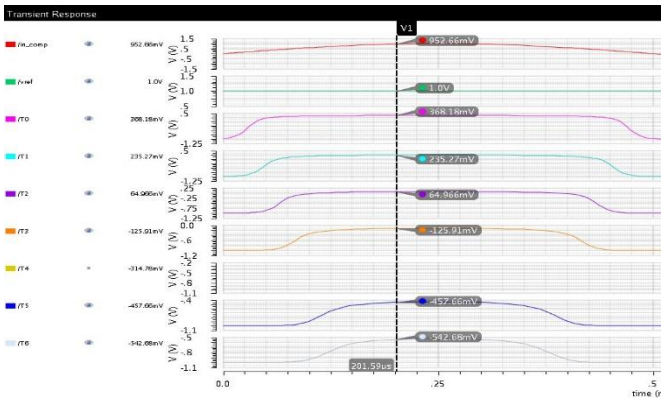

Fig. 6 Comparator transient response

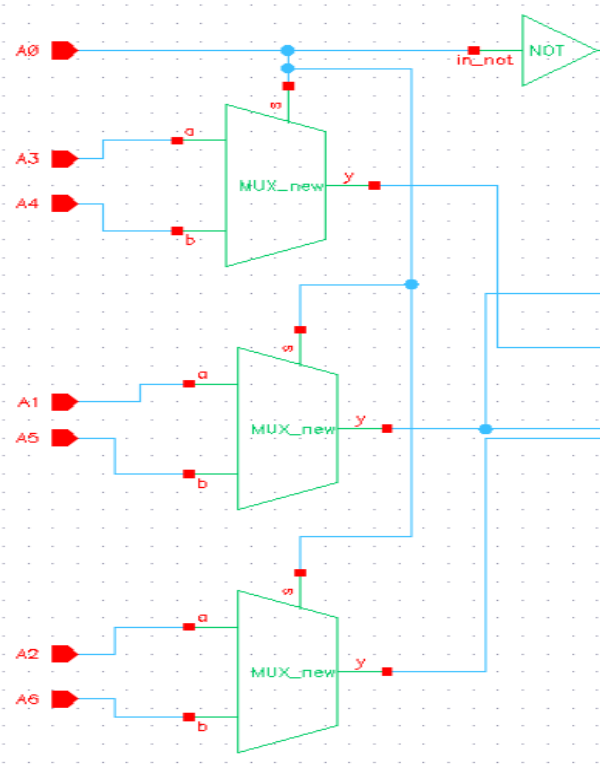

Fig. 7 Encoder

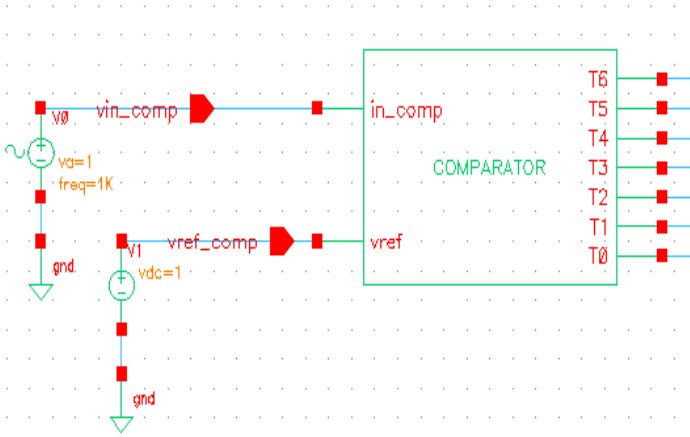

Fig. 8 3 Bit Flash ADC schematic

3.Pipeline ADC

Each stage pipeline ADC can be designed presented in fig. 9 [14-15]. The sample-holdcircuit produces the sampled signal of the input. It is sent through flash ADC to convert the input signal into 3 bits. These 3 bits will be reconstructed back into analogue form. The difference of the input signal and the reconstructed signal will produce the residue output signal. This residue signal is than feed into next stage of ADC. Fig. 9 presents first stage pipeline ADC schematic. Cadence spectre based transient response of first stage pipeline ADC in fig. 11;Table 1 lists the input signal at different time and their output after each stage

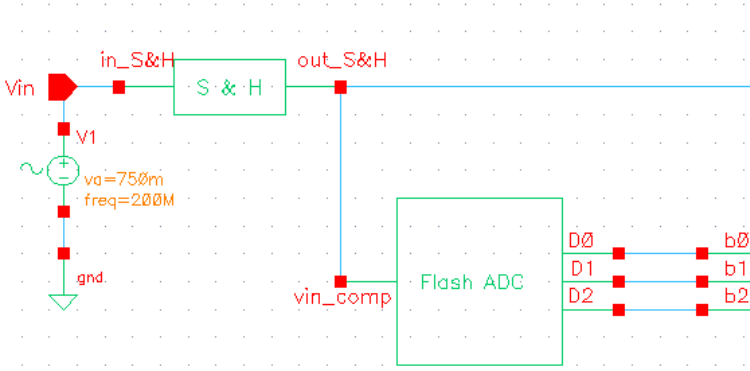

Fig. 9 First stage of pipeline ADC

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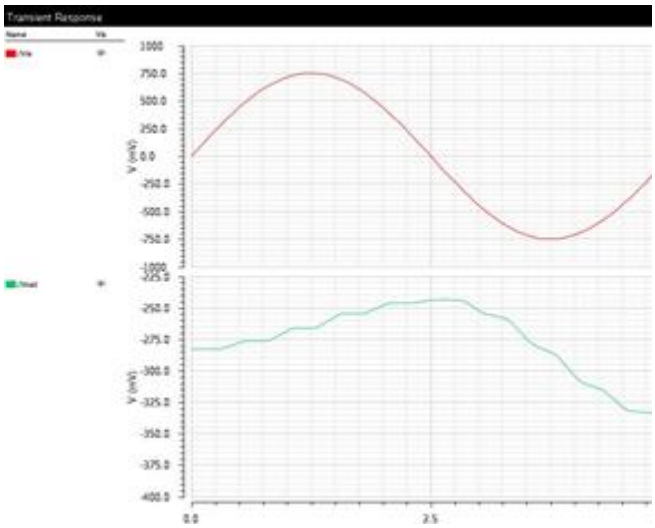

Fig. 11 Transient response of first stage pipeline ADC

Table ITransient analysis of input and output signals

Time (ns)	Vin (mv)	Vout (mv)
0	0	-280.0
1.25	750	-265.0
2.5	0	-245.0
3.75	-500	-287.5
5	0	-335.0
6.25	750	-320.0

4. Conclusion

If the required sampling rate ranges in megaHz than pipelined ADC is the most suitable architecture. Use of Flash type converters in pipelined ADCwill help to attain high speed, high resolution, and low power all together. Pipelined ADCs have its wide range of applications, majorly in digital communication anddigital signal processing. In this work, first stage of pipeline ADC has been designed which gives 3 bits as output. As multistage pipelined ADC has several similar first stage pipelined ADCs, were each stage produce 3 output bits in this design. In 6 stages pipelined ADC we will be having 18 output bits but single bit will be discarded in each stage due to digital error correction block, resulting in final 12 bits as output.

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