THINK INDIA JOURNAL

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

Performance Analysis of Top Contact SG-OTFT and Bottom Contact SG-OTFT Structures

Akshara Rana
Department of Electronics and Communication Engineering
Lovely Professional University Jalandhar-144411, INDIA
aks.ranaakshara@gmail.com

Abstract— *The characteristics of the Organic transistor incorporating the Single gate structure of the OTFT is been done and the performance comparison have been successfully simulated and compared for both the BGTC and BGBC structures. Few of the parameters using Top contact OTFT have been found better like high current ratio enabling it to make superior displays like e-paper., Also, device characteristics for the BGTC OTFT has been found better as compared to that from BGBC structure, the circuit employing it shows better performance. The circuit of display pixel could further utilize the above mentioned work and can be fabricated for large display applications for constituting organic emissive displays. For most of the useful applications, low-cost manufacturing is accompanied with high-performance, reproducibility, and stability of devices.Here the performance analysis of OTFT using all the structures of OTFT is done which can be further used this OLED-OTFT composed device into the pixel circuitry for smart phones, smart watches, Television and tablet applications that has been aimed here is to provide flexibility to the circuit as it is an all organic device along with reduction of the threshold voltage and the power consumption of the circuit.*

Keywords—Organic Thin Film Transistor, Single Gate- OTFT, Dual Gate-OTFT, Organic Semiconductor, Organic LED

I. Introduction

The traditional MOS transistors have four terminals whereas Organic transistors is free of the fourth terminal,i.e. Body, that enables it free from body effect. Also formation of accumulation layer is whole sole responsible for the current conduction in Organic transistors unlike the MOSFETs where current conduction takes place later on after the accumulation formation, i.e. the formation of inversion layer.

Various structures of OTFT have marked the importance associated to various performance parameters. The structures are classified on the basis of the location of the terminals Drain, Source, Gate along with the placement of the Organic semiconductor layer that takes place in charge conduction. Novel structure comprising the Single gate structure has marked very remarkable performance which is further being improved taking into account the other structures of OTFT like Dual gate, vertical channel based, cylindrical channel OTFT. Structures of Single gate OTFT can be further divided on the basis of the location of the gate ,i.e. Top gate and bottom gate. Top gate structure is nearly same as that of MOSFET and are expensive to fabricate and thus less preferred since the OSC layer may be contaminated due to very high rise in temperature at any time, also the adhesion may also be very weak .

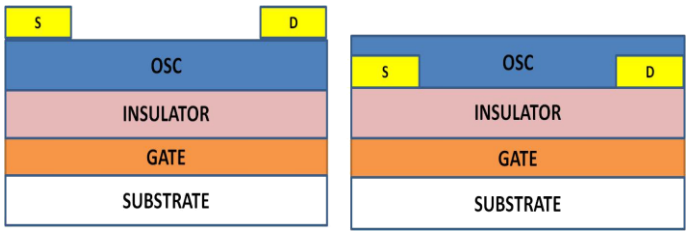


Fig. 1. Bottom gate Top Contact and Bottom contact structures

The DG-OTFT structure is a bit different from the single gate, as it has one more gate located at the bottom with insulator, S/D contacts, OSC and then top gate insulator. Here the bottom gate takes part in the charge accumulation that enables the current conduction.The other gate on the top accelerates this channel conductivity with the external bias supplied to it. Hence V_T can be further controlled in much more wider range but at an extra fabrication cost and

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

the extra gate material cost as well. But this brings highly controlled operation of OTFT leading to higher current, steeper subthreshold slope, and a good control of V_T. The bias can be applied to DG-OTFT in different ways depending on the application requirement. One is the bias to be provided to the top gate keeping the bottom gate grounded, and vice versa, and the other could be the external bias to be provided to both the gates at the top and bottom leading to the formation of two conducting channel in the active layer.

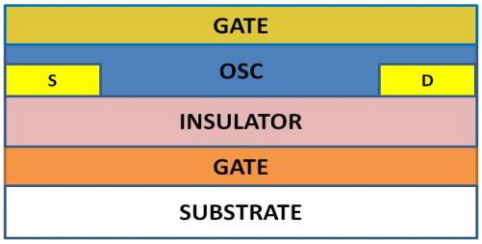


Fig. 2. Dual gate structure.

This work is categorized into five areas, considering the present basic Section I. From that point, Section II depicts the reenactment arrangement used to examine the presentation of SG-OTFT and various structures on the basis of top contact and bottom contacts. Segment III portrays electrical trademark and parameter extraction of the Single Gate. Segment IV describes the characteristics obtained after simulation. At long last, Section V outlines significant results and applications of the proposed work.

II. Simulation Setup

The objective of the section is to analyze the characteristic differences of the bottom gate structures for both the top contact and bottom contact devices. The performance device structure is been formed using Atlas-2D Silvaco TFT Device simulator. Thereafter, in the upcoming section, characteristics based on the transfer curve and output curve are obtained later on and analyzed by using Atlas-2D Silvaco TFT Device Simulator.
The simulation structures of SG-OTFT device for which the comparison has been made on the basis of the position of the contacts i.e. top contact or bottom contact. Structural Parameters used herein are mentioned in the tabulated form thereafter.

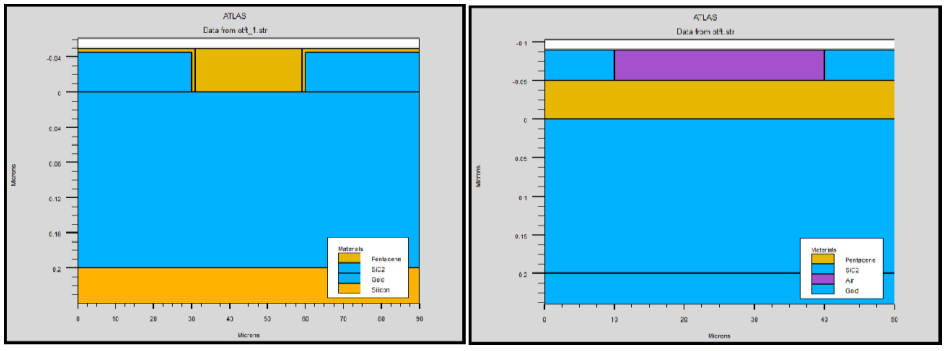


Fig. 3. Simulated structures of single gate (a) BGBC and (b) BGTC devices.

The performance of the bottom contact devices is generally substandard to the top contact OTFT devices. The reason behind this difference is typically concluded by the contact resistance that is developed in the interface contact barrier of the organic semiconductor layers in the region of the pre-patterned source and drain metal layers. Both of the structures, BGBC and BGTC, uses various device parameters as listed in table 1.1 as follows. The channel length and channel width remains same for both. The only difference arises in the thickness of Pentacene.

III. SG-OTFT ELECTRICAL CHARACTERISTICS AND PARAMETER EXTRACTION

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

The materials which are used in the OTFT device are mentioned in the table below. The device dimensions and the type of materials used are also specified.

Table I. Structural parameters used in the device study.

Device Parameters	**Device Dimensions**		**Materials**
	BGTC	**BGBC**	
Channel Length L (μm)	30	30	-
Channel Width W (μm)	1000	1000	-
Insulator Thickness (nm)	200	200	Silicon Dioxide
OSC Thickness(nm)	40	50	Pentacene
S/D Thickness (nm)	4/40	4/40	Titinium/Gold
Gate Thickness (nm)	25	25	Heavily Doped Silicon

The energy band gap signifies the amount of energy required to energize hole or electron to jump from corresponding valence band to the subsequent conduction energy band. The dielectric constant refers to the permeability of the insulator material which signifies how faster the charge carrier can accumulate near the surface. Here the electron mobility is smaller as compared to that of the holes mobility since the semiconducting material is of Pentacene that is of *p-type* material. Larger the channel length, higher is the hole mobility. The BGTC possess the larger conducting channel length as compared to that of BGBC. The work function for the electrode materials must be sufficiently high so as to minimize the required threshold voltage. The doping concentration signifies the conducting mechanism of the device. Higher the inserted impurity and thus doping concentration, lesser is the threshold voltage.

Table II. Electrical properties of different layers in the device study.

Electrical Properties	**Pentacene (OSC)**	**SiO_2 (Dielectric)**	**Gold (S/D Electrodes)**	**Silicon (Gate)**
Band Gap (eV)	2.2	-	-	-
Dielectric Constant	-	4	-	-
Mobility of electron (cm^2/Vs)	5e-5	-	-	-
Mobility of hole (cm^2/Vs)	1.5e-4	-	-	-
Work Function (eV)	-	-	5.1	3.9

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

Doping Concentration (cm^{-3})	-	3.06×10^{13}	-	1e21

Extraction of Performance Parameters is done here. The application of the organic transistor depends on various parameters. These significant parameters are described as follows along with the formulae used during simulation.

1) High mobility

$$\mu = \mu_0 \left(V_{GS} - V_{TH} \right)^{\alpha} \quad (1)$$

Here, μ_o specifies OSC band mobility taken at very small V_{gs} around 0.5V. Then, α is usually specified between 0.2 to 0.5 that depends on dielectric permittivity, doping density and conduction mechanism of the device in active material.

2) Small value threshold voltage

$$V_T = \frac{q.N_A.t_{OSC}}{C_{OX}} \quad (2)$$

Where t_{OSC} is the thickness of the OSC layer around 40 to 50 nm, q is the charge, N_A is the doping concentration, and C_{OX} is the capacitance associated with the silicon dioxide layer

3) High on/off current ratio

$$I_{ON}\ I_{OFF} = \frac{C_i \mu (V_{GS} - V_T)^2}{(t_{OSC}\ V_{DS}\ \sigma)} \quad (3.1)$$

$$I_{OFF} = \left(\frac{W}{L} \right) t_{OSC} V_{DS} \sigma \quad (3.2)$$

Here ,σ signifies channel conductivity, *L, W are* the channel length and width respectively, C_i implies gate dielectric capacitance per unit area.

4) Steep sub-threshold slope

$$SS = \left(\frac{\partial V_{GS}}{\partial \log_{10}(I_{DS})} \right) \quad (4)$$

The ratio terms are change in gate biased voltage and the drain current.

For both the BGBC and BGTC OTFT devices in the study, the various performance parameters are tabulated as follows in Table 1.3. Their comparison clearly shows that the BGTC OTFT device has the better performance in terms of higher drain current and lower threshold voltage.

IV. COMPARISON OF SG-OTFT STRUCTURES AS TOP CONTACT AND BOTTOM CONTACT

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

All the parameters are calculated for voltage given to gate that ranges from -5V to -20V keeping drain voltage at -20V. The top contact configuration found improved performance with respect to bottom contact as there are very few morphological disorders found in active layer. BGBC configuration found 62% reduced mobility due to large value of contact resistance. Also the BGTC configuration offers low contact resistance as there is a huge area for injecting the charge carriers that provide increased current value. In addition to this, it is observed that bottom contact structure posses higher sub-threshold as compared with top contact due to formation of a lower mobility area around contacts which led to rise in the trap density.

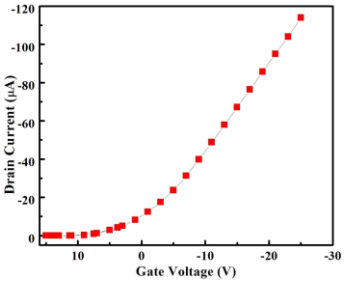
Table III. Extracted performance parameters for both the configurations-BGBC and BGTC of OTFT.

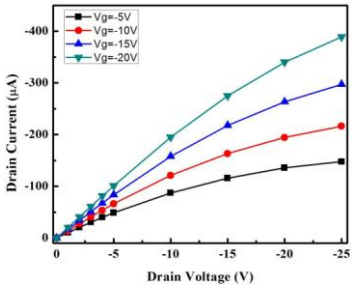
Performance Parameters	**Data**	
	BGTC	**BGBC**
Current (I_D)	4e-4 A	1.6e-4 A
Mobility (μ_{sat})	8.14e-13 cm^2/Vs	1.6e-13 cm^2/Vs
On-Off Current Ratio (I_{on}/I_{off})	817.96	1.7e3
Threshold Voltage(V_T)	-5 V	-11 V
Subthreshold Slope(SS)	10.96 V/A	14.0926 V/A

All the parameters are calculated for V_G ranging from -5V to -20V, keeping V_D at -20V. The top contact configuration found improved performance with respect to bottom contact as there are very few morphological disorders found in active layer. BGBC configuration found 62% reduced mobility due to large value of contact resistance. Also the BGTC configuration offers low contact resistance as there is a huge area for injecting charge carriers that provide increased current value. In addition to this, it has been seen that bottom contact structure posses greater sub-threshold as compared with top contact since lower mobility area is formed around contacts which led to rise in the trap density.

V. SIMULATED CHARACTERISTICS FOR BOTH TC AND BC SG-OTFT

The output curves (a) Transfer Characteristics (Id-Vg), and (b) Output Characteristics (Id-Vd) of the simulated device for the top contact and bottom contact configuration is shown in Fig. 3.2 and Fig. 3.3 respectively.





ISSN: 0971-1260
Vol-22-Issue-17-September-2019

Fig. 4. Output curves (a) Transfer characteristics, and (b) Output characteristics for BGTC configuration of the device under study.

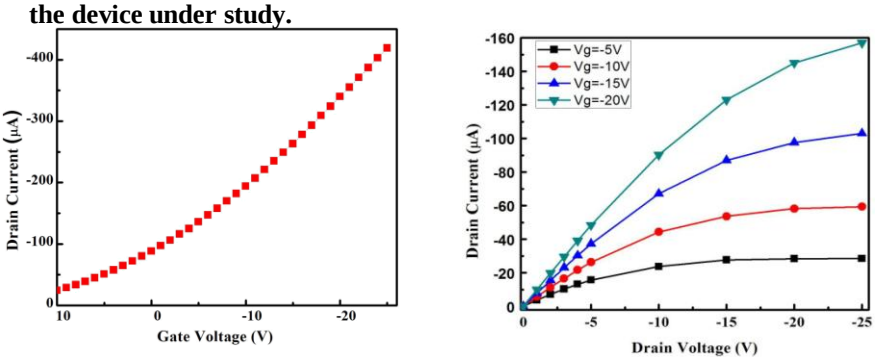


Fig.5. Output curves (a) Transfer characteristics, and (b) Output characteristics for BGBC configuration of the device under study.

For both the transfer and output characteristics, all the parameters are calculated for the gate voltage ranging from -5V to -20V, and the drain voltage of -20V. The top contact structure exhibit higher performance than bottom contact as there are very few morphological disorders in active layer.

The output curve shown in Fig. 4. clearly signifies the larger drain current for the Bottom Gate Top Contact Configuration as compared to that shown in Fig. 5. The transfer characteristics are obtained at the drain voltage of -20V and the gate voltage of -5V. The output drain characteristics are obtained for different gate voltages varying from -5V to - 20V.

VI. CONCLUSION AND FUTURE SCOPE

The section concludes the performance comparison of the single gate structures for both the top contact and bottom contact configuration on the basis of the simulated device structure and the transfer and output characteristics. Device behavior solely depends on dopant concentration. The device structure is not only the single way for better device making. Along with device structure the process of fabricating the OTFT devices and the properties of the material play a crucial part. Though the bottom contact devices lags in performance but their flexibility and low cost makes appropriate choice for display applications.

OTFTs are used to make flexible displays incorporating the organic LEDs in their circuit. Light-emitting organic field-effect transistors (LEOFETs) have additionally been utilized to consolidate the OLED optical yield with the controlled gate voltage of the OTFT in one single device, however it's been settling on the expense of the device yet causing it to perform better and adaptability likewise makes the device to be progressively prominent, as no backplane is required.

VII. REFERENCES

[1] D. Gupta, M. Katiyar, and D. Gupta, "An analysis of the difference in behavior of top and bottom contact organic thin film transistors using device simulation", *Organic Electronics* 10 , 775-784, 2009.

[2] B. Kumar, B.K. Kaushik, and Y. S. Negi, "Organic Thin Film Transistors: Structures, Models, Materials, Fabrication, and Applications: A Review", *Polymer Reviews*, vol. 54, no. 1, pp. 33-111, Feb. 2014.

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

[3] J. Kovac, L. Peternai, and O. Lengyel, "An Organic Light-Emitting Diode with Field-Effect Electron Transport", *Thin Solid Films, 433,* pp. 22–26, 2003.

[4] M. Pope, H. Kallman, and P. Magnante, "Electroluminescence in Organic Crystals", *J. Chem. Phys.*, vol. *38,* pp. 2042-2043, 1963.

[5] C.W. Tang, and S.A. VanSlyke, "Organic electroluminescent diodes'', *Appl. Phys. Lett.,* vol. *51*, no. 12, pp. 913-915, 1987.

[6] J. H. Burroughes, D. D. C. Bradley, A. R. Brown, R. N. Marks, K. Mackay, R.H. Friend, P. L. Burns, and A. B. Holmes, "Light emitting diodes based on conjugated polymers'', *Nature, 347,* pp. 539-541, 1990.

[7] C. Hosokawa, K. Fukuoka, and H. Kawamura, "Improvement of Lifetime in Organic Electroluminescence'', *SID Digest,* vol. *35,* pp. 780-783, 2004.

[8] W. M. Tang, U. Aboudi, J. Provine, R. T. Howe, and H. S. P. Wong, "Improved Performance of Bottom-Contact Organic Thin-Film Transistor Using Al Doped HfO_2 Gate Dielectric", IEEE Transactions on Electron Devices, vol. 61, no. 7, July 2014.

[9] P. Broms, J. Birgersson, N. Johansson, M. Lögdlund, and W. R. Salaneck, *Synth. Met., 74,* pp. 179-181, 1995.

[10] Fgg Schon, J. H.; Batlogg, and B. "Trapping in organic field-effect transistors", *J. Appl. Phys., 89*(1), 336–341, 2001.

[11] Halik, M. Klauk, H. Zschieschang, U. Schmid, G. Radlik, and W. Weber, "Polymer gate dielectrics and conducting polymer contacts for high performance organic thin film transistors", *Adv. Mater., 14*(23), 1717–1722, 2002.

[12] T. Cui, and G. Liang, "Dual gate pentacene organic field-effect transistors based on a nanoassembled SiO2 nanoparticle thin film as the gate dielectric layer", *Appl. Phys. Lett., 86*(6), 064102-1–064102-3, 2005.

[13] M. Maccioni, E. Orgiu, P. Cosseddu, S. Locci, and A. Bonfiglio, "Towards the textile transistor: Assembly and characterization of an organic field effect transistor with a cylindrical geometry", *Appl. Phys. Lett., 89*(14), 143515-1–143515-3, 2006.

[14] H. W. Zan, and K. H. Yen, "Vertical channel organic thin-film transistors with meshed electrode and low leakage current", *Jpn. J. Appl. Phys., 46*(6A), 3315–3318, 2007.

[15] D. J. Gundlach, L. Zhou, J. A. Nichols, T. N. Jackson, P. V. Necliudov, and M. S.

Shur, "An experimental study of contact effects in organic thin film transistors", *J. Appl. Phy., 100*(2), 024509-1–024509-13, 2006.

[16] H. Klauk, "Organic thin-film transistors", *Chem.Soc.Rev., 399*(7), 2643–2666, 2010.

[17] X. A. Zhang, J.W. Zhang, W. F. Zhang, and X. Hou, "Fabrication and comparative study of topgate and bottom-gate ZnO–TFTs with various insulator layers", *J. Mater. Sci. Mater. Electron., 21*(7), 671–675, 2010.

[18] M. F. C. Luo, I. Chen, and F. C. Genovese, "A thin film transistor for flat planel displays", *IEEE Trans. Electron Devices, 28*(6), 740–743, 1981.

[19] H. C. Tuan, M. J. Thompson, N. M. Johnson, and R. A. Lujan, "Dual gate a-Si: H thin film transistors", *IEEE Electronic Device Lett., 3*(12), 357–359, 1982.