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A Novel Method For Fault Coverage And Routing Path Delay Reduction In GDI Logic Design

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ABSTRACT: Small Delay Defects are introduced for high quality performance in the industry. Various ATPG tools will produce the timing information to select the longest path. In this paper, a novel method for fault coverage and routing path delay reduction in GDI logic design. Due to timing requirements in GDI design, the new scheme is introduced to detect the delay faults effectively. By extracting the common paths in the circuit, the number of nodes will be reduced. The fault coverage and routing path will perform its operation depend on the circuit. This system will propagate the faults by using routing procedure. Small delay defects will produce high fault coverage to overcome this routing procedure is introduced. The fault coverage and routing path delay design will reduce the low faults coverages compared to SDD. This system will exploit the characteristics of GDI circuitry to enable the applications of test pattern circuitry.

KEY WORDS: Small Delay Defects (SDD), Automatic test pattern generation (ATPG), fault coverage, routing path delays, CMOS, GDI (GATE DIFFUSION INPUT).

I. INTRODUCTION

In order to adopt the delay defects in the system, transition delay fault model is used. Extra delays in the circuit will be obtained because of some manufacturing defects. These manufacturing defects are resistive opens and resistive bridges. To detect the small delay defects mainly transition faults are generated from tests. Hence at the fault location a transition delay fault model is assumed. To create logic errors at the circuit outputs, small delay defects must propagate the long paths. But various numbers of approaches are introduced to reduce the small delay defects. Here mainly three categories are discussed in detail manner.

Firstly timing aware automatic test pattern generation is introduced using commercial tools. In this timing aware automatic test pattern generation there are two delays mainly cell delay and net delay. This TA-cell format will extract the files by finding a path and this gives high delay for propagating the delay effect from targeted node. In this TA-ATPG, the high delay test coverage is used. High CPU time and high pattern count is required in ATPG system. In order to find long paths in fault generation large amount of timing information is used. Test compatibility is very low in ATPG system. In TA-ATPG, the pattern volume and process time is reduced and faults in the system are identified [2].

Up to now TA-ATPG method is discussed, let us discuss about the N-bit detection of transition delay fault (TDF-ATPG) method. The TDF-ATPG is used to detect the fault for N multiple times. Huge pattern counts are required to detect the faults for N times. To detect the small delay defects pattern selection method is introduced. Same pattern is used to detect the tests for pattern count. Various pattern selection methods are introduced to consider the tradeoff between N-Detect tests and 1-detect tests. By using this tests efficient pattern is introduced to reduce the smaller delay defects [5-6].

The last category introduced to reduce the smaller delay defects is path delay fault ATPG (PDF-ATPG). Various critical paths are introduced to generate the test and detect the critical paths. This system will mainly defect the small fraction path delay paths in effective way.

Small delay defects will be reduced using new test generation method [7]. This method will detect the fault models like PDF ATPG, TA-ATPG and TDF-ATPG. By using all this techniques we can generate the long paths using high pattern quality. PDF-ATPG is used to conduct the test for high timing variability paths. The both TA-ATPG and TDF-ATPG paths will cover the test when it is not connected. Because of this effective results are obtained compared to PDF-ATPG method. Hence the newly generation

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method will generate the test patterns depend on some challenges like

(1) Low delay test coverage
(2) High pattern volume and
(3) High ATPG run time

This newly test generation method will reduce the small delay defects and it obtains the high DTC with compact test patterns. For each small delay defect the newly generation method will extract the path system in effective way. SDD will pass the long paths in each stem of the small delay defect. User defined fault model is introduced to add some test conditions at the path stems. This process will be commercial at the ATPG system and it archives high compact ability. To get high DTC the stems will pass the pattern in standard format. Hence low test pattern counts are obtained using new generation method. Along with that, the new generation method will produce low delay test coverage compared to other methods.

The small delay defect will reduce the delay according to the given pattern format. But here the overall impact is very critical in TA-ATPG method. Compared to others the path delay uses long time clock periods. Here the circuit and incorrect results are obtained in the system. By using least slack paths, the detection of SDD become very simple and it will excite the faults in effective way. False paths and multiple cycle paths are obtained by using longest paths in the circuit. Lumped delay effect is obtained in the system using transition delay fault.

To excite the transition delay, TDF model is used and it will use the shorter paths in effective way. Here TA-ATPG method is introduced for grow interest in SDD. ATPG patterns make effectively longer paths to get high rated clock frequencies. The timing information is supplied using standard delay format. This will scan the file using static timing analysis method. But limited number of files is introduced. Cross talk, power supply noise and account process variations are extended depend on the format chosen. Longest paths are designed to prone the SDD.

II. SDD GENERATION

The stem based fault transformation model will transform the problem to detect the small delay defect. This small delay defect will use the user defined fault model to obtain commercial output. Basically, the ATPG tool will obtain high delay test coverage for small delay defects. Let us consider this with an example. A and B are used in the sub section part. Coming to A, it will determine the path stem concept effectively and B will determine the paths for sharing long stem for each SDD. This will give entire information how to detect the long paths in SDD. The user defined fault model will determine the transformation to transfer the paths in effective way. This TDFs will improve the probability of small delay defects by passing longer paths.

Here the propagation of fault effects of SDD will be introduced to get high DTC. This is mainly used in the longest path. The length of propagation path will determine the faults by choosing shortest paths. The propagation of longest path will define the pattern format and resulting to consider the compact the test patterns. Hence, the path stems will be extracted using path stems from path propagation.

To generate the compact test pattern, SDD should be detected. From figure (1) the all TDFs are generated using SDD list. In the left part, the SDD will determine the longest path and produce the time by using fault location. By using long paths, the path stem will define a particular location. Udf will be used to transform the path stem and fault location
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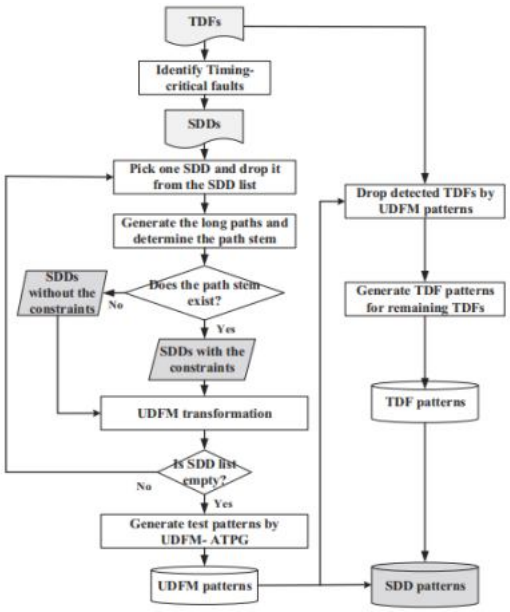

Fig. 1: SDD FLOW GRAPH

The test generation flow in Figure 1, which is called "Proposed Method 1 (PM1)" in our experiments, attempts to generate test patterns that propagate the fault effect through the corresponding path stem for each SDD. However, due to ATPG limitation and circuit function limitation, some test conditions at the

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path stem may not be satisfied during test generation and hence the corresponding SDD may not be detected. To solve this problem one may use TDF-ATPG to generate test patterns for these undetected SDDs. This however will result in lower DTC for these SDDs. We thus propose another test generation flow, which is called "Proposed Method 2 (PM2)" in our experiments, for these low DTC SDD faults as described next.

From above figure (1), the test generation flow graph is shown. The test generation flow will delay with small delay defects with low DTC. In the targeted list the SDD will pick up the threshold D1 and it defines the threshold effective way. Here TA-ATPG will generate the targeted small delay defects. High quality pattern set is obtained by using pattern selection method. Compared to others, the small delay defect count is executed based on additional patterns.

III.RELATED WORK

The testing criteria of the rising low power and fast correspondence computerized flag preparing chips can be tends to investigate the very much designed profound submicron transistor advancements. The execution of the fundamental number circuits to actualize complex calculations, for example, convolution, relationship and advanced sifting, characterizes the execution of numerous greater modules of Digital Signal Processors (DSPs). The semiconductor business has seen a touchy development of mix of modern interactive media based applications into portable hardware gadgetry since the most recent decade. Be that as it may, control utilization is the basic region of worry in this field and must be diminished for a specific working recurrence. Also, there is a drive by creators to take a stable at littler silicon territory, higher speed, longer battery life, and upgraded dependability in light of dangerous development of interest and prominence of convenient electronic items.

The motivation behind coordinated hardware is to pack complex electronic circuits in least territory with decrease in power dispersal and postponement. With the period of innovative progression, diminishing the quantity of transistors and ultra-low power configuration has turned into the main thrust for mix of an ever increasing number of uses without acquiring any overhead as far as silicon region. The execution of configuration is significantly represented by three essential variables viz. zone multifaceted nature, postpone execution and consistency of interconnection.

The consistency of interconnection implies the manner in which transistors are set down, directing of interconnects in the most ideal way and conforming of format. Territory of the circuit likewise relies upon the interconnection of wires which exhaust the greater part of the region of a VLSI circuit. Diverse rationale styles have been proposed throughout the years with an exchange off of one execution angle to the detriment of other. The circuit delay is influenced by the quantity of transistors in arrangement, wiring interconnections identified with wiring capacitances, transistor sizes and number of reversal levels. Full adder usage can be accomplished by utilizing it is possible that one rationale style or more than one rationale style.

The XOR-XNOR circuits are fundamental building hinders in different circuits' particularly number juggling circuits (adders and multipliers), blowers, comparators, equality checkers, code converters, mistake recognizing or fault remedying codes and stage identifier. The adders and multipliers being the quick number continuously calculation cells and generally utilized for some circuits of VLSI configuration are the regular research zones. A further expansion to unwavering quality and fault issue issues have been brought with the ascent up in chip thickness and increment in power utilization of VLSI frameworks. Building and cooling cost of VLSI frameworks likewise runs up with high power dispersal. These days, low power utilization alongside least postponement and zone necessities is one of vital plan thought for IC originators.

Circuit acknowledgment for low power and low territory has turned into a vital issue for the development of incorporated circuit towards exceptionally high joining thickness and high working frequencies. Because of the imperative pretended by XOR and XNOR gates are obtained in different circuits particularly in number continuously circuits, improved plan of XOR and XNOR circuit to accomplish low power, little size and low deferral is required. The essential circuit to plan XOR-XNOR gate is to get low power utilization and postponement in the basic way and right yield having the least number of transistors to execute the voltage swing. XOR gate is a basic building square of advanced circuits and there is constant research proceeding to upgrade its execution.

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Along these lines, from its origin the structure of XOR gates frames the fundamental building square of all advanced VLSI circuits which has been experiencing a significant enhancement, being spurred by three essential plan objectives, viz. limiting the transistor tally, diminishing the power utilization and expanding the speed. Hosseinzadeh underscored that the circuit execution can be enhanced through transistor tally minimization. XOR gates assume an imperative job in advanced frameworks including math circuits, encryption circuits, comparator, equality checker, etc. Upgrading the execution of the XOR gates can altogether enhance the execution of these circuits. Many plan structures and procedures have been created to plan XOR gate with decrease in power utilization. The writing study uncovers a wide range of XOR gates that have been acknowledged throughout the years. The predominant to structure XOR gate is to procure right yield voltage swing with least number of transistors and furthermore, execution with low power utilization and postponement in the basic way

IV. EXISTING SYSTEM

The below figure (2) demonstrates the design of existed framework. The non full-swing circuit which is appeared as far as productive. This structure has a yield voltage drop issue for just single information legitimate esteem of it's besides. To tackle this issue and give an ideal structure to the gate of the circuit, in the circuit appeared in Fig. 1 was existed. In the full swing the structure of the yield of this, the all conceivable info mixes. The basic way of the circuit on gates does not have of the existed system of gate operation.

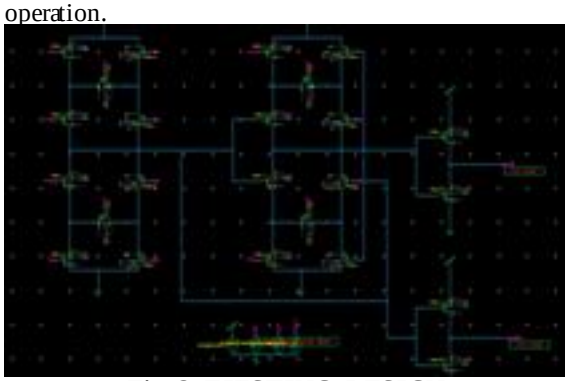

Fig. 2: EXISTING DESIGN

The data sources are as per the following A and B which are denoted as the capacitances of the XOR circuit. These sources are not symmetric on the grounds side and one of these two should be related with the commitment of AND gate. In the same way another should be related with the scattering of nMOS transistor. In addition, the data capacitances of transistors N2 and N3 are not equal in the perfect situation (least PDP).

Generally, the information relationship with transistors N2 and N3 won't impact the limit of the circuit. Hence, it is more brilliant to relate the data A, which is moreover connected with the passages and to the transistor with smaller information capacitance. By doing this, the information capacitances are progressively symmetrical, and thusly, the delay and power usage of the circuit will be lessened. To light up which transistor (N2 or N3) has greater data capacitance, let us consider the condition that the wellsprings of information change from AB = 00 to AB = 10.

V. PROPOSED SYSTEM

Fig. 3: PROPOSED DESIGN

The above figure (3) shows the design of proposed system. The full adder comprises of 10 transistors are used entirely in the system. The creators give gates to enhance the execution of full adders. These gates give awful yield rationale levels for certain information blends. This issue can be tackled by controlling the (W/L) proportions of PMOS and NMOS transistors, which reestablishes the rationale levels to a worthy dimension. Basically, the gates used in this will produce the intensity in the full adder cell. Hence the power utilization is decreased by the full adder cell with the planning. The gates will be used in different computerized applications. In this system we use eight transistors for better purpose. Here NOT gate is used in the circuit of grounds of NOT cells. These cells should drive the delay in basic formation level.

Depend on the logic style of transistor the circuits operate its function. In this circuit the power utilization is superior. The signals are mainly associated with the full adder circuits. The circuit will

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contribute its signals by using multiplexers. Consequently, two concurrent signs with a similar postponement are important to keep away from glitches in the yield hubs of the FA. In this structure, the yields have been driven just by nMOS transistor, and along these lines, two pMOS transistors are associated with yields as cross coupled to recoup the yield level voltages.

The main issue in the circuits is having cross coupled structure. This structure will expand the intensity of the system. Not only intensity, the measure of transistor is also expanded to a level. By using two NOT gates in the system is a big issues in the system. Hence the outputs of GDI will practically diminish the output stage. But the proposed system gives effective results compared to existed system.

VI. RESULTS

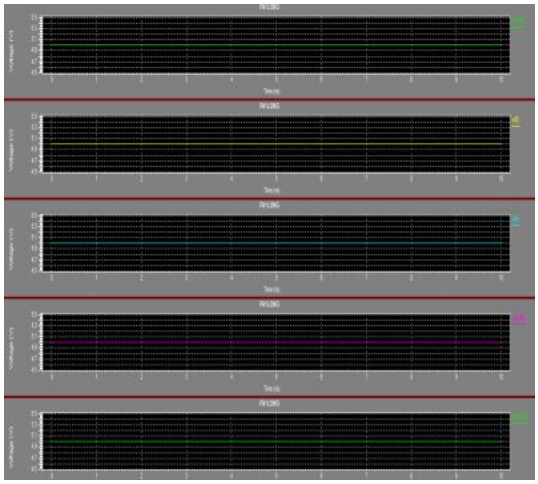

Fig. 4: EXISTED OUTPUT WAVEFORMS

S.NO	CMOS DESIGN	GDI DESIGN
Total Number of Nodes	17	10
Independent nodes	12	5
MOSFET's	24	10

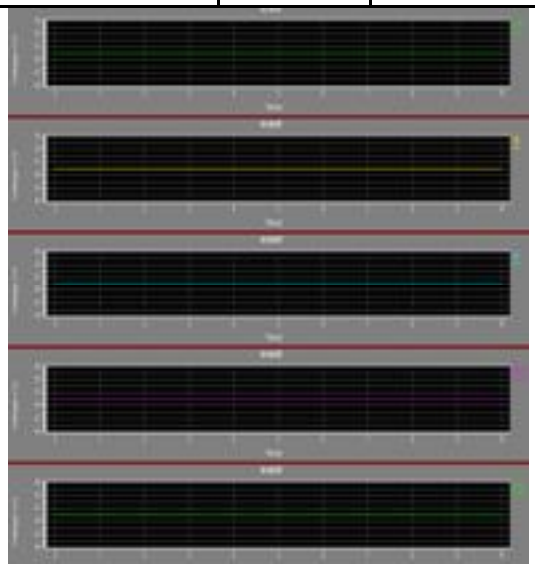

Fig. 5: PROPOSED OUTPUT WAVEFORMS

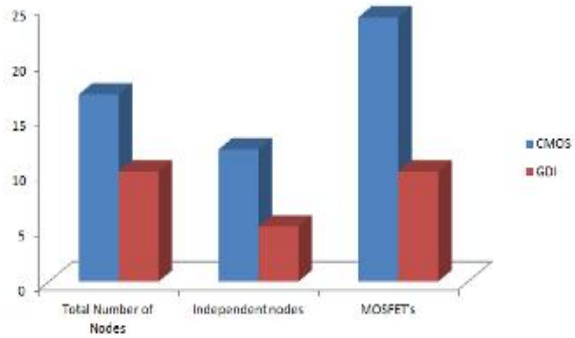

Fig. 6: COMPARISON GRAPH

The above figure (6) shows the comparison graph of independent nodes, total nodes and number of MOSFET's available. Compared to the design of CMOS, the GDI design gives effective output.

Table. 1: COMPARISON TABLE

VII. CONCLUSION

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In this paper, we propose a novel method for fault coverage and routing path delay in GDI logic design. This system is depending on the path stem. In SDD the test conditions are based on determined path stems and ATPG will be constrained to propagate fault effects through path stems. Here the fault paths will be determined using long paths. By using the novel method higher-quality and more efficient patterns can be generated by our method. The proposed technique reduces the problem of path delay fault testing for scan based designs of path delay fault testing with complete accessibility to the combinational logic, and thus minimal area overhead. The scheme also provides significant reduction in number of nodes during scan operation.

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