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High Speed Dual Mode Logic

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Abstract: Dual Mode Logic also termed as DML, as its name indicates it has two modes namely static and dynamic mode. Dual Mode Logic is mainly divided in two topology which is Type A topology and Type B topology. This research paper includes the analysis of many of the combinational circuit like NOR , NAND, XOR, different combinational circuit with 3 inputs that is $(\bar{A}.\bar{B})+\bar{C}$, $(\bar{A}+\bar{B}).\bar{C}$ and $(\bar{A}+\bar{B}).(\bar{B}+\bar{C}).(\bar{C}+\bar{A})$ to achieve a generalized way so that we can use Type A and Type B thoughtlessly in the circuit. Due to DML techniques increases the battery life as there is reduction in power dissipation as compare to all other circuits.

I. INTRODUCTION

Power dissipation is one of the major concerns of VLSI circuit designs for which DML is primary technology. To achieve the optimize circuit having low power dissipation and delay optimization we have work on DML concept because it effects the power dissipation of almost all circuits. Dual Mode Logic also termed as DML, as its name indicates it has two modes.

- Static mode
- Dynamic mode.

In DML we connect an additional transistor to the output of the standard CMOS circuit to optimize the delay and power dissipation in the circuit by varying the width of the additional transistor. The output of the circuit varies according to the asynchronous clock pulse applied to the gate of the external transistor. DML is basically divided in two topology that is Type A topology and Type B topology.

In type A topology of Dual Mode Logic a PMOS is connected to the output of standard CMOS circuit and the gate of PMOS is connected to a clock which is asynchronous with respect to input of the standard CMOS circuit. For type A topology the DML will work in static mode if the clock provided to the PMOS is constant with positive pulse that is with voltage 3V or logic 1 while for dynamic mode the clock will be varying asynchronously with respect to input that is the pulse period for both the input and the clock will be different. For dynamic mode of type A topology the output will be recorded for only the positive edge of clock because for the negative edge of clock PMOS acts as a pull up resistor. In type B topology of Dual Mode Logic Inverter a NMOS is connected to the output of Inverter and the gate of inverter is connected to a clock which is asynchronous with respect to input of the inverter. For type B topology the DML will work in static mode if the clock provided to the NMOS is with voltage 0V or logic 0. For dynamic mode the output of the DML inverter will be recorded for only negative edge of clock because NMOS is in OFF state for the negative edge while for dynamic mode of type B topology the output will be recorded for only the negative edge of clock because for the positive edge of clock NMOS acts as a pull down resistor.

The structure of the basic DML gate is shown below is very simple consisting of orthodox CMOS gate adding Pre-Discharge transistor to it. When the transistor behaves in static mode, the transistor is active and operating in the same way as the standard CMOS one. DML works as Type A or Type B which is also shown in the figure.

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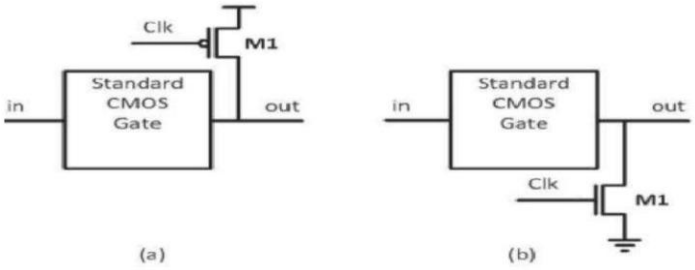

Fig. 1 Type A and type B topology

Our objective of this paper is to achieve low power dissipations during circuit operation and increasing the speed of the circuit by reducing the delay between input and output. It can only be possible with the help of DML because according to measured difference between the power consumption and delay optimization for standard CMOS and DML logic circuit. Thus our aim is to reduce the power dissipation and optimize the delay by the means of some application such as Type A and Type B in DML.

A. Static DML (standard CMOS logic operation)

Static logic circuit provides adjustable implementation of logic function based on steady-state behaviour of standard CMOS circuit. The standard logic gate generates its output levels when we apply the power supply and input to the circuit. Checking the power dissipations and time delays between the inputs and outputs implements that depending upon the size of the circuit. Power dissipations is low but the time delay is high in static case or standard CMOS operation. In static case there is no effect of additional transistor as it is not active as clock is unable to make the transistor on. Some of basic features are

- Output impedance is low while input impedance is high.
- Low in Power consumption.
- Noise margins are high.
- Between VDD and GND there is no fixed path.

B. Dynamic DML

In dynamic mode of operation, the additional transistor which is attached to the standard CMOS logic circuit comes into play. The clock pulse provided to additional transistor making the transistor ON which affects the output of the standard CMOS along with that it also effect the power dissipations and time delay of standard CMOS logic circuit. It is done by changing the width of the additional transistor which affects the mobility of the transistor.

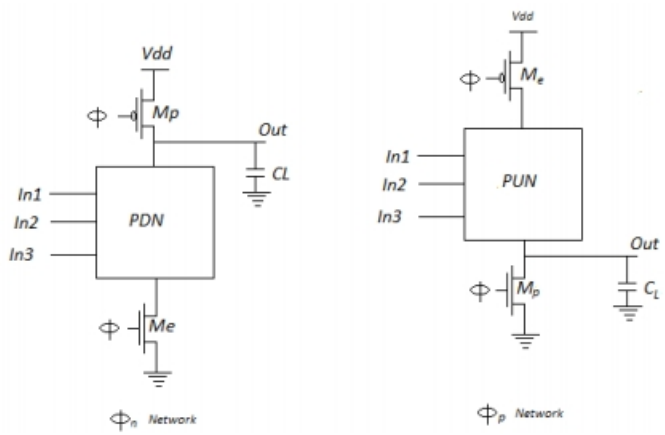

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Fig. 2 Dynamic WorkingofDML

II. DESIGN AND IMPLEMENTATION

A. Type A Inverter

In type A topology of Dual Mode Logic Inverter a PMOS is connected to the output of Inverter and the gate of inverter is connected to a clock which is asynchronous with respect to input of the inverter.

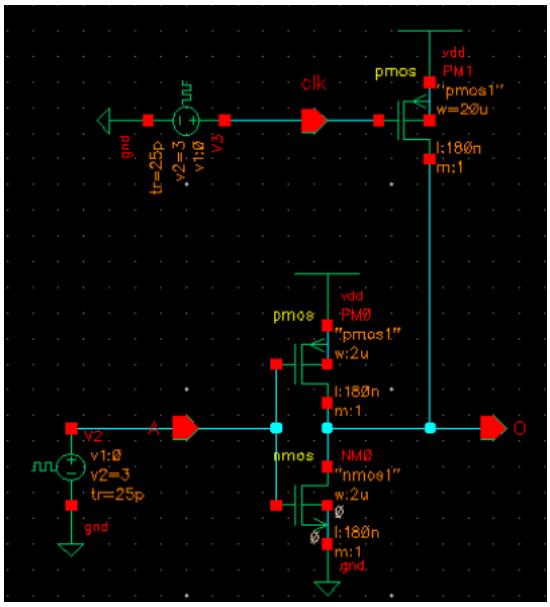

Fig. 12 DML Inverter type A topology

Initially the channel width of both the PMOS and a NMOS is 2 micro meters that is it is the default configuration of all the transistors with channel length as 180 nano meter. Since DML has two modes-:

- Static mode
- Dynamic mode.

For type A topology the DML will work in static mode if the clock provided to the PMOS is constant with positive pulse that is with voltage 3V or logic 1.

Table 6 Values for clock for static mode type A

Vpulse for clock	
Voltage 1	3V
Voltage 2	3V
Period	10ns
Rise time	25ps
Fall time	25ps
Pulse Width	5ns

In static mode the clock is logic 1 that the input to the gate of PMOS is logic 1 or 3V so the PMOS is always in OFF state therefore the output of the DML inverter will not be affected by the external PMOS and the output will follow the universal rule that is if IN=1, OUT=0 and vice versa. As the static mode is different

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from dynamic mode but the output of inverter will be same in both the mode so there will be difference in power dissipation and delay therefore the power consumption and delay is calculated and it is as follows

Table 7 Power and Delay in static mode type A

Power	10.85 µW
Delay	18.66 ps

The delay which is calculated is the time taken for obtaining output after the input is applied.

For dynamic mode of DML the clock provided to the external PMOS must be varying asynchronously with the input of the standard CMOS inverter. The output of the DML inverter will be recorded for only positive edge of clock because PMOS is in OFF state for the positive edge as logic 1 is applied to the gate of the PMOS while for negative edge logic 0 is given to the gate of PMOS which in turn put the PMOS in ON state so it act as a pull up resistor and VDD is the output for the whole DML inverter.

Table 8 Dynamic mode for type A inverter

Input	clk	Output
3.0V	1	534.96 nV
3.0V	0	69.32 mV
0V	1	3.0V
0V	0	3.0V

The output of the type A DML inverter is similar to the basic inverter circuit for the positive edge of clock while for negative edge of clock the output will be 3.0 V irrespective of the input but for input 3V and clock 0 the output is 69.32 mV which is violation of the basic rule for PMOS so to overcome this problem we decided to increase the channel width of the external PMOS from 2µm to 20µm. We proposed the 20µm width after doing the parametric analysis for the circuit and the 20µm width is the feasible as compare to other value of channel width.

Table 9 Dynamic mode for type A inverter (width 20µm)

Width	Input	clk	Output
20µm	3.0V	1	3.15µV
20µm	3.0V	0	2.75V
20µm	0V	1	3.0V
20µm	0V	0	3.0V

Since the performance in dynamic mode is high as compare to static mode but the power is more in dynamic mode.

Table 10 Power and Delay in dynamic mode type A inverter

Power	1.71mw
Delay	9.78 ps

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B. Type B Inverter

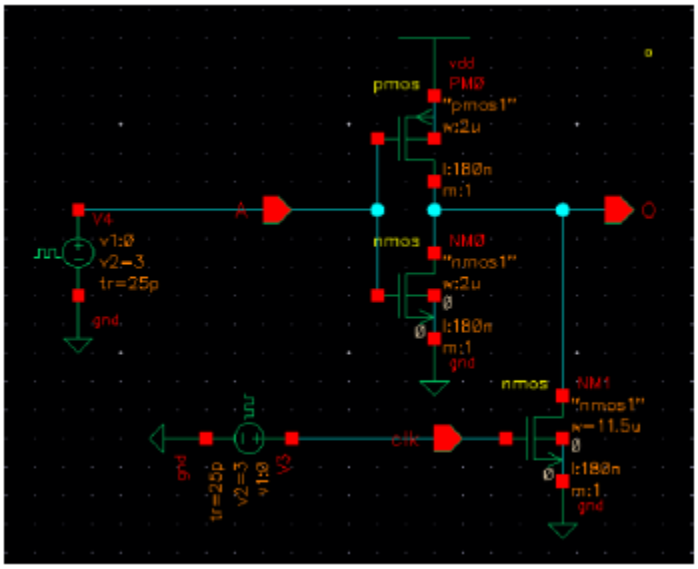

Fig. 16 DML inverter type B topology

In type B topology of Dual Mode Logic Inverter a NMOS is connected to the output of Inverter and the gate of inverter is connected to a clock which is asynchronous with respect to input of the inverter. Initially the channel width of both the NMOS and a PMOS is 2 micro meters that is it is the default configuration of all the transistors with channel length as 180 nano meter. For type B topology the DML will work in static mode if the clock provided to the NMOS is with voltage 0V or logic 0. The values for the clock pulse for the static mode in type B topology will be same as the values for the clock pulse in type A topology except the Voltage 1 and Voltage 2 value which will be 0V as NMOS will be in OFF state.

In static mode the clock is logic 0 that the input to the gate of NMOS is logic 0 or 0V so the NMOS is always in OFF state therefore the output of the DML inverter will not be affected by the external NMOS and the output will follow the universal rule that is if IN=1, OUT=0 and vice versa.

Table 12 Power and Delay in static mode type B inverter

Power	10.61 µW
Delay	18.20 ps

For dynamic mode the output of the DML inverter will be recorded for only negative edge of clock because NMOS is in OFF state for the negative edge as logic 0 is applied to the gate of the NMOS while for positive edge logic 1 is given to the gate of NMOS which in turn put the NMOS in ON state so it act as a pull up resistor and GND is the output for the whole DML inverter.

Table 13 Dynamic mode for type A inverter

Input	clk	Output
3.0V	1	2.06 µV
3.0V	0	3.50 µV
0V	1	313.52 mV
0V	0	3.0V

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The output of the type b DML inverter is similar to the basic inverter circuit for the negative edge of clock while for positive edge of clock the output will be 0 V irrespective of the input. To increase the performance of the circuit we increased the width of the external NMOS initially the width of the external NMOS is 2µ meter, so we increased the width from 2µm to 11.5µm and then recorded the power and delay of the circuit.

III. RESULT AND ANALYSIS

The static mode and dynamic mode of a Dual Mode Logic circuit can be differentiated by power dissipation of the circuit and the performance of the circuit. In static mode the power dissipation is low while the performance is moderate. And in dynamic mode the power dissipation is high with high performance In all the circuit which is included in this paper, it is clearly seen that in static mode the power consumption is low but the delay between the input and output is high while in dynamic mode the power consumed by the circuit is more but the delay between all the input and output of the circuit is less, so the performance of the circuit increases which means that the time taken by the circuit for performing some task is less which is the primary goal for designing any circuit in this century. In dynamic mode the power increases because the transistor which is attached externally with the circuit is come into play as the input to it is variable that is the clock given to PMOS/NMOS is in pulse from (0-LOW, 1-HIGH) while in static mode the transistor gets the constant input that is the clock is constant HIGH for PMOS and LOW for NMOS so the external transistor always remains in OFF state that why the power dissipation is low in static mode.

IV. CONCLUSION

Today Dual Mode Logic is very popular method in designing the circuit with low power consumption and high speed evaluation. This paper consists of some of the combinational circuits which are made using DML method on which the analysis is done to see the difference in the static and the dynamic mode and a „Thumb rule‟ is proposed so that we can use type A or type B topology just by seeing the circuit. In NAND type A topology the power consumption is less as compared to its type B topology. But for NOR type A topology the power consumption is more with respect to its type B topology. For all other circuits the type B topology is better as compared to type A in case of power consumption (All the analysis is done in cadence 180 nm technology). Thumb Rule-: If there are all the product terms then type A topology is better while if there is a single sum term then type B topology is better.

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