THINK INDIA JOURNAL

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

Comparative Analysis of FinFETs Device on Technology Scale of 14nm vs 20nm

Shekhar Verma[1], Suman Lata Tripathi[1], Nitin Kumar[2]

[1]School of Electronics & Engineering,
[2]School of Computer Science Engineering
Lovely Professional University,Punjab, India.
Email: shekhar.14572@lpu.co.in

***Abstract*—**In comparison to MOSFET much superior in terms of Electrostatic properties and manufacturability. In today scenario FinFETs are acknowledged as the most promising technology for developing the low power based VLSI Circuit. Most challenging aspect in the MOSFET designing to scale down the device to below 20nm but this challenge can easily overdrive by using the FinFET for minimizing the leakage current to enhance the performance of the VLSI circuits. In this paper, proposed a two design of FinFETs at scale of 20nm & 14nm in terms of channel length and comparative analysis done on the performance basis. In 14nm FinFETs 81% improvement observed as compared to 20nm and 81.6% improvement observed in terms of power parameter and I_{on} /I_{off} current ratio of the 14nm FinFET is 10^{10} in compared to the 20nm FinFET. Switching speed of the 14nm FinFET high in comparison to 20nm.

***Keywords*—**Very Large Scale Integration, Drain Induced Barrier lowering, Subthreshold, Oxide thickness, Channel Length, Short channel effect, mobility, Drift Current, electrical characteristics, Complementary Metal-Oxide-Semiconductors (CMOS). FinFET, high- K dielectric material, threshold voltage.

1. INTRODUCTION

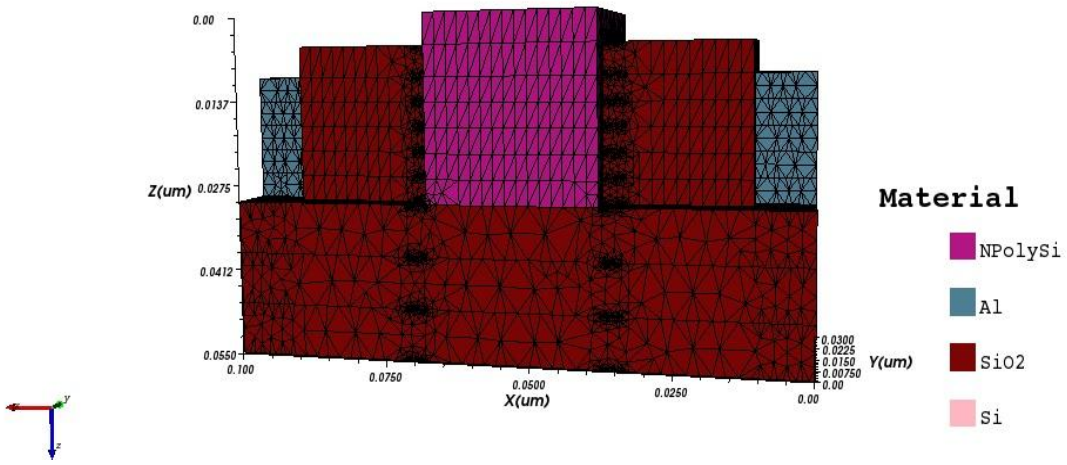
In now days, challenging aspect is to reduce the size of the device that degraded the performance of the VLSI Circuit. As we decreases the size of the device then one factor, leakage current more dominant that effect on the short channel effect in the circuit. This issue more dominant in MOSFET device as its scale done on below 45nm. To overcome this challenge, FinFETs act as a most promising technology for developing the low power based VLSI circuit [1]. To suppress the leakage current, in FinFET device channel can be cover from all around through the gate terminal that restrict the flow of off current when device in saturation region [2]. By using of high-k/metal gate material enhance the performance of the FinFETs at a next level. Scaling down of the transistor in terms of channel length from 45nm to 7nm is possible due to FinFET. FinFET provide a better controllability over the channel through the gate terminal by introducing the concept of the Multi-gate. In FinFETs, designer can easily design the double or multigate gate or gate around configuration on the device to scale down the transistor size. In short- channel length device, short

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

channel effect more dominant due to reduce in the space between the source terminal and drain terminal of the device [3].This paper distributed on the four section. In first section we discuss the introduction part and second section based on the literature review. In third section we describe the result discussion & device configuration and in last section we concluded the paper.

2. REVIEW OF THE LITERATURE

In long channel device, short channel effect is not more dominating but as we scale down the transistor size this effector play an important role. In short channel device, as we reduce the distance between the source and drain terminal then off current increasing more rapidly in cut-off mode that enhance the short effect in the device[4]. To minimize this issue, multigate terminal come into a picture by placing the multiple gate around the channel length of the device. This type of structure, introduced the concept of the FinFETs technology [5]. To suppress the leakage current in the FinFETs device, introduce the usage of the high- k material of dielectric for the gate terminal [6]. With the help of the high-k material of dielectric efficiently suppress the short channel effect in the FinFET device [7]. By usage of the high metal work function for the contact terminal leads to higher efficiency of the circuit and boast up the performance of the device [8]. By the changing the shape of the fins from triangular to trapezoidal leads to enhancing the performance of the device [9].



ISSN: 0971-1260
Vol-22-Issue-17-September-2019

FIGURE 1 FINFET OF 20NM CHANNEL LENGTH

3. RESULT DISCUSSION & DEVICE CONFIGURATION

A. Proposed Design Structure and material composition

We designed the FinFET device on the scale of 14nm and 20nm by using the Visual TCAD by the Cogenda. In both the design we used the same material so that fair comparison will be done in terms of performance of the device. Table 1 shown the configuration of the both the design.

TABLE 1:Proposed FinFET Parameter

S.No	Structural Parameter	Value
A	Device Width (nm)	13
B	Fin Height of the Device (nm)	11 to 13
C	Device Doping Concentration (/cm^3)	10^{15} to 10^{20}
D	Oxide Thickness (nm)	3 to 4

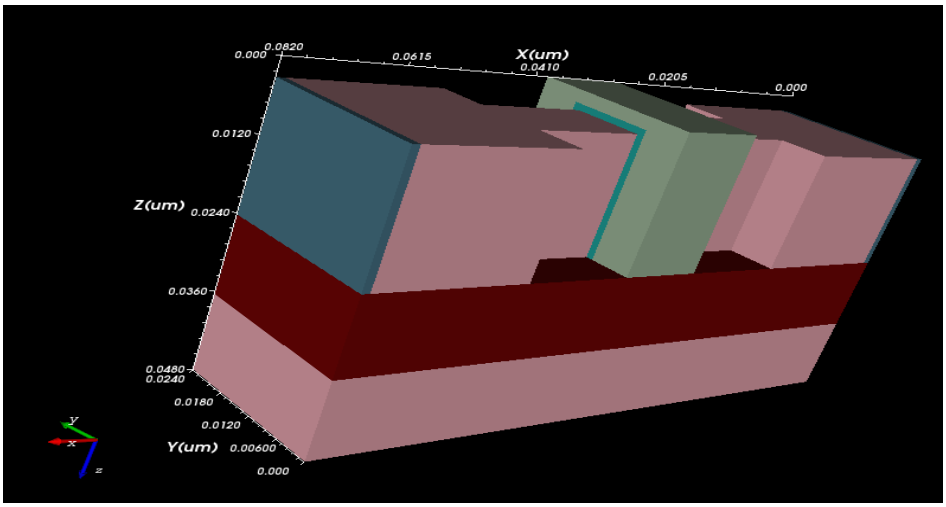


Figure 2 FinFET of 14nm Channel Length

Figure 2, shown the pictorial view of the 14nm FinFet that designed on the Visual TCAD. Both the design simulated on the same experimental condition for analyzing the performance of the proposed FinFET device. We vary the current of drain terminal from 0 to 1 V with Step of 0.05 V so that many points can be

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

recorded. While doing the simulation for the proposed design we kept the temperature of the device at 300 K and drain voltage at 1V.

B. Result Discussion

We simulated both the design from 0 to 1 V at step of 0.05 V for analyzing the Gate voltage vs. drain current at 1 V value of drain voltage.

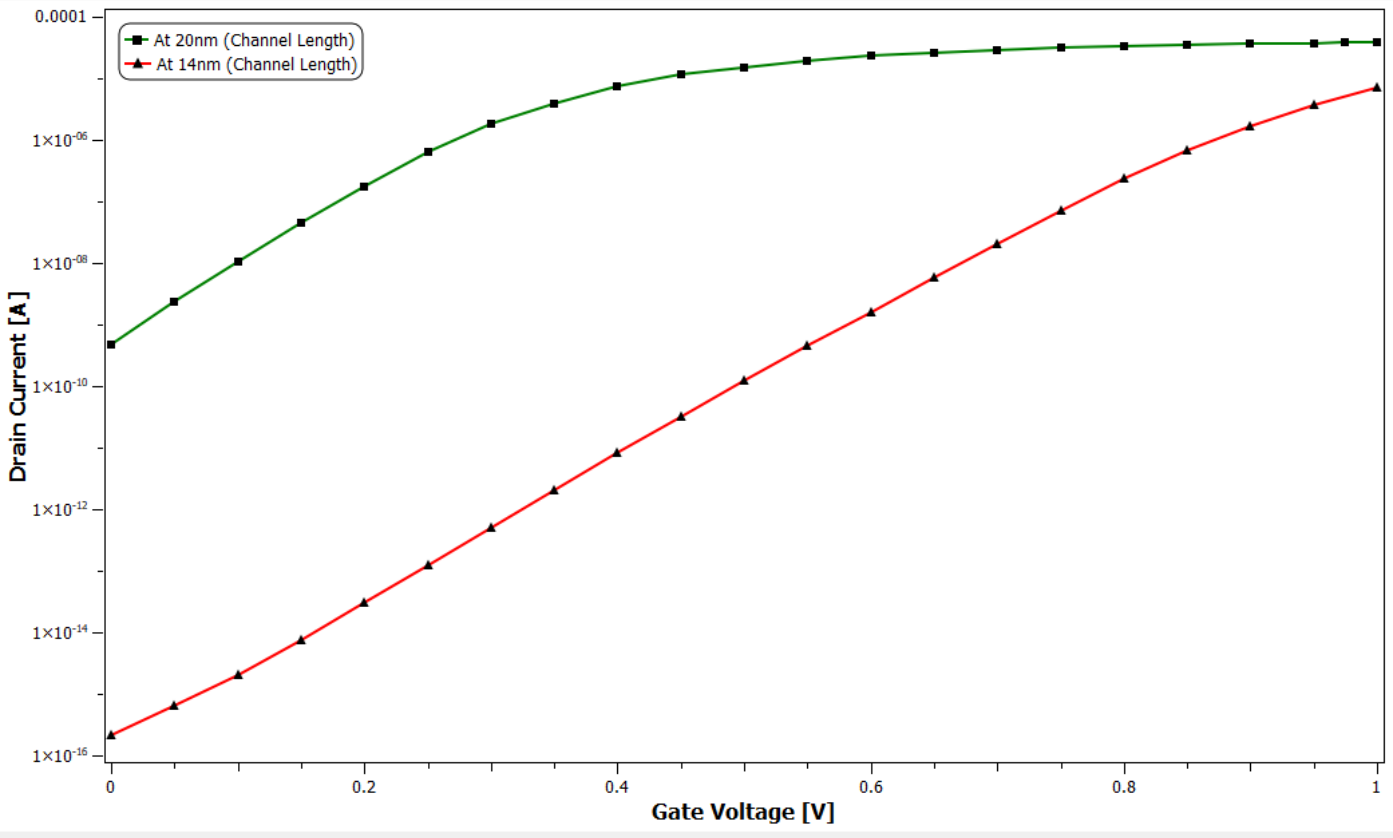


Figure 3. Gate Voltage vs. Drain Current at V_{ds} (1V)

TABLE II: Comparison of Gate Voltage Vs Drain Voltage

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

Gate Voltage	Drain Current (A)	
	At 20nm	At 14nm
0	4.77E-10	2.14E-16
0.05	2.32E-09	6.25E-16
0.1	1.05E-08	2.02E-15
0.15	4.45E-08	7.44E-15
0.2	1.77E-07	3.02E-14
0.25	6.28E-07	1.24E-13
0.3	1.78E-06	5.04E-13
0.35	3.93E-06	2.04E-12
0.4	7.33E-06	8.11E-12
0.45	1.14E-05	3.15E-11
0.5	1.52E-05	1.19E-10
0.55	1.92E-05	4.42E-10
0.6	2.29E-05	1.61E-09
0.65	2.62E-05	5.78E-09
0.7	2.89E-05	2.05E-08
0.75	3.12E-05	7.09E-08
0.8	3.31E-05	2.32E-07
0.85	3.48E-05	6.74E-07
0.9	3.63E-05	1.68E-06
0.95	3.76E-05	3.62E-06
1	3.86E-05	7.06E-06

As per Table II and figure 3, we can analyze the performance of both design. In case of 14nm FinFET, off current and on current values in comparison to 20nm on higher side. For analyzing the performance of any device I_{on} current and I_{off} current are two crucial parameter for identifying the electrical characteristics of the device. In case of 14nm, off current values is 10^{-16} and on current values is 10^{-6}. As per the on current and off current values, in 14nm design current ratio values also higher that's is 10^{10} that boast up the switching speed of the device.

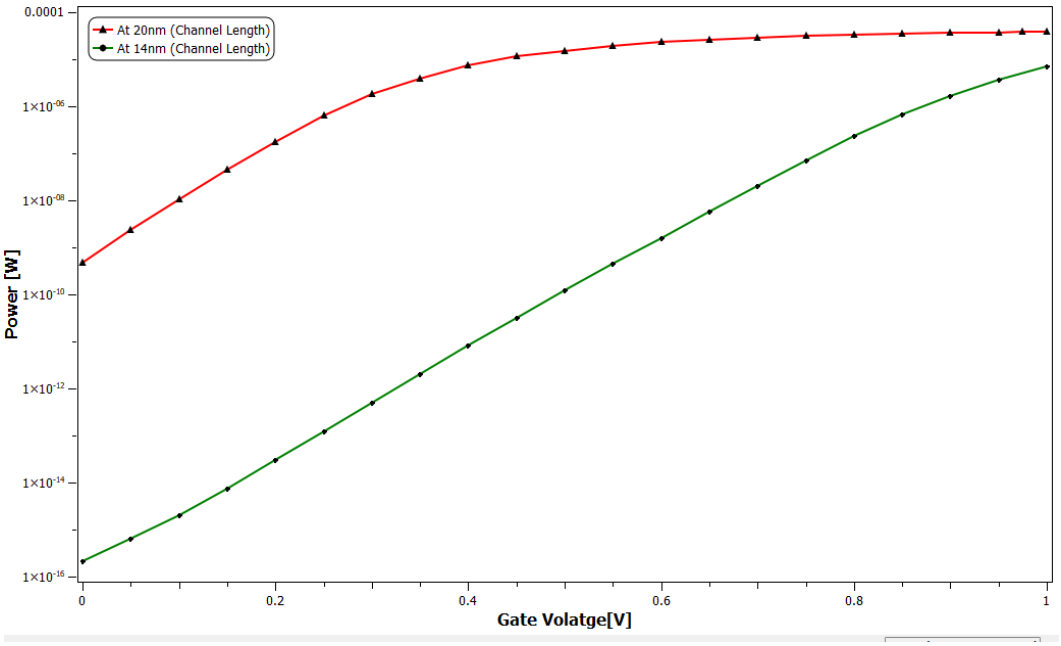


Figure 4. Power vs. Gate Voltage at V_{ds} (1V)

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

As per figure 4, we can analyze this, power dissipation is minimum in 14nm device in comparison to 20nm FinFET. This is due to lesser value of the off current in saturation region that leads to minimum short channel effect and reduces the leakage current.

4. CONCLUSION

In the paper, in this paper, proposed a two design of FinFETs at scale of 20nm & 14nm in terms of channel length and comparative analysis done on the performance basis. In 14nm FinFETs 81% improvement observed as compared to 20nm and 81.6% improvement observed in terms of power parameter and I_{on}/ I_{off} current ratio of the 14nm FinFET is 10^{10} in comparison to the 20nm FinFET. Switching speed of the 14nm FinFET high in comparison to 20nm.So 14nm device we can use for designing of IOT based applications.

REFERENCES

[1] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," IEEE Trans. Electron Devices, vol. 49, no. 1, pp. 112–119, Jan. 2002. doi: 10.1109/16.974757.

[2] S. E. Tyaginov, M. I. Vexler, A. F. Shulekin, and I. V. Grekhov, "Statistical analysis of tunnel currents in scaled MOS structures with a non-uniform oxide thickness distribution," Solid-State Electron., vol. 49, no. 7, pp. 1192–1197, 2005. doi: 10.1016/j.sse.2005.04.007

[3] A. R. Brown, J. R. Watling, A. Asenov, G. Bersuker, and P. Zeitzoff, "Intrinsic parameter fluctuations in MOSFETs due to structural nonuniformity of high-□ gate stack materials," in Proc. Int. Conf. Simulation Semiconductor Processes Devices, Sep. 2005, pp. 27–30. doi: 10.1109/SISPAD.2005.201464.

[4] Tripathi, S.L. & Patel, G.S., "Design of Low Power Si0.7Ge0.3 Pocket Junction-Less Tunnel FET Using Below 5 nm Technology" Wireless Personal Communication (2019), pp.1-10. https://doi.org/10.1007/s11277-019-06978-8

[5] G. S. Patel, S. L.Tripathi "Performance Enhnaced Unsymmetrical FinFET and its Applications" IEEE EDKCON, pp.222-227, 2019

[6] S.L.Tripathi, S.Verma, N.Dhanda"Characterisation of Ultra-Small Pocket Si0.7Ge0.3 Junction-less Tunnel FET with SOI" Devices for Integrated Circuit (DevIC), pp. 79-83, 23-24 March, 2019, Kalyani, India

[7] S.Verma, S. L.Tripathi, M.Bassi "Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications" Devices for Integrated Circuit (DevIC), pp.84-88, 23-24 March, 2019, Kalyani, India

[8] S L Tripathi, R.Mishra, R A Mishra, "Characteristic comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm technology" IEEE ICPCES, pp.1-7, December, 2012

[9] Book chapter on "Low Power High Performance Tunnel FET: Analysis for IOT applications" IGI global publisher, ISBN:9781522595748, pp.47-57

[10] H. Nam and C. Shin, "Study of high-k/metal-gate work-function variation using Rayleigh distribution," IEEE Electron Device Lett., vol. 34, no. 4, pp. 532–534, Apr. 2013. doi: 10.1109/LED.2013.2247376.

[11] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D 'atomistic' simulation study," IEEE Trans. Electron Devices, vol. 45, no. 12, pp. 2505–2513, Dec. 1998. doi: 10.1109/16.735728.

[12] S. R. Stiffler, R. Ramachandran, W. K. Henson, N. D. Zamdmer, K. McStay, G. La Rosa, K. M. Boyd, S. Lee, C. Ortolland, and P. C. Parries, "Process technology for IBM 14-nm processor designs featuring silicon-on-insulator FinFETs," IBM J. Res. Develop., vol. 62, nos. 2–3, pp. 11:1–11:7, Mar./May 2018. doi: 10.1147/JRD.2018.2800518.

[13] J. H. Lee, Y. M. Shcu, C. C. Wu, Y. M. Liu, Y. C. Chou, and S. C. Chin, "An electrical failure analysis (EFA) flow to quantitatively identify invisible defect on individual transistor: Using the characterization of random dopant fluctuation (RDF) as an example," in Proc. IEEE Int. Symp. Phys. Failure Anal. Integr. Circuits (IPFA), Jul. 2018, pp. 1–5.doi: 10.1109/IPFA.2018.8452513.

[14] T. Grasser, "Stochastic charge trapping in oxides: From random telegraph noise to bias temperature instabilities," Microelectron. Rel., vol. 52, no. 1, pp. 39–70, Jan. 2012. doi: 10.1016/j.microrel.2011.09.002.

[15] B. Kaczer, J. Franco, M. Cho, T. Grasser, P. J. Roussel, S. Tyaginov, M. Bina, Y. Wimmer, L. M. Procel, L. Trojman, F. Crupi, G. Pitner, V. Putcha, P. Weckx, E. Bury, Z. Ji, A. De Keersgieter, T. Chiarella, N. Horiguchi, G. Groeseneken, and A. Thean, "Origins and implications of increased channel hot carrier variability in nFinFETs,"in Proc. IEEE Int. Rel. Phys. Symp., Monterey, CA, USA, Apr. 2015,pp. 3B.5.1–3B.5.6. doi: 10.1109/IRPS.2015.7112706.

ISSN: 0971-1260
Vol-22-Issue-17-September-2019

[16] A. Rahman, J. Dacuna, P. Nayak, G. Leatherman, and S. Ramey, "Reliability studies of a 10nm high-performance and low-power CMOS technology featuring 3rd generation FinFET and 5th generation HK/MG," in Proc. IEEE Int. Rel. Phys. Symp. (IRPS), Mar. 2018, pp. 6F.4-1–6F.4-6. doi: 10.1109/IRPS.2018.8353648.

[17] P. Paliwoda, Z. Chbili, A. Kerber, T. Nigam, K. Nagahiro, S. Cimino, M. Toledano-Luque, L. Pantisano, B. W. Min, and D. Misra, "Selfheating effects on hot carrier degradation and its impact on logic circuit reliability," IEEE Trans. Device Mater. Rel., vol. 19, no. 2, pp. 249–254,Jun. 2019. doi: 10.1109/TDMR.2019.2916230.

[18] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, and C. Fiegna, "Characterization and modeling of hot carrier-induced variability in subthreshold region," IEEE Trans. Electron Devices, vol. 59, no. 8, pp. 2093–2099, Aug. 2012. doi: 10.1109/TED.2012.2200683.

[19] E. R. Hsieh, S. S. Chung, C. H. Tsai, R. M. Huang, C. T. Tsai, and C. W. Liang, "New observations on the physical mechanism of Vthvariation in nanoscale CMOS devices after long term stress," in Proc. Int. Rel. Phys. Symp., Apr. 2011, pp. XT.9.1–XT.9.2. doi: 10.1109/IRPS.2011.5784610.

[20] S. S. Chung, "The process and stress-induced variability issues of trigate CMOS devices," in Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits, Jun. 2013, pp. 1–2. doi: 10.1109/EDSSC.2013.6628181.