*THINK INDIA JOURNAL*

ISSN: 0971-1260

Vol-22-Issue-17-September-2019

# POWER, AREA AND DELAY BASED COMPARATIVE ANALYSIS OF DIFFERENT FULL ADDERS BASED ON REVERSIBLE LOGIC

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***Abstract- The importance of reversible logic is increasing day by day and beseeming more salient logic in terms of optimized delay and power based output and has been integrated into a number of applications these days such as Low Power VLSI, DNA Computing, Bio Informatics and many more. Earlier, the major reason of power dissipation was used to be the loss of bits of information i.e. The garbage bits during the procedure of logical operations, but this problem can be minimized accompanying reversible gates as it involves one –to – one mapping of input and output vectors which results in reduction of garbage bits. Along with that, as the full adder is the essential part in most of the digital computerised logics, so the comparison between different reversible gates based 1 bit full adder to find out the most efficient circuits with respect to, LP (Leakage Power), DP (Dynamic Power),Area and Delay (Worst Path) is presented in this paper. The RTL examination was completed utilizing Cadence Tool for Area, Delay and Power at 45 nanometre and 90 nanometre innovation for both slow and fast libraries.***

***Index Terms— Garbage output, Reversible, Constant input***

## I. INTRODUCTION

To understand the reversible logic, first of all, we need to understand the difference between reversible and irreversible logic. In digitally logical systems, we use of 0's and 1's series the information is represented with the series of level 1's to represent an erudition. Agreeing to C.H. Bennett [2], each bit appears with the energy of KTln2 with T refers to the absolute temperature and k refers to Boltzmann constant and if we consider the concept given by Landauer [1] which employs that the system consist of (nx1) i.e. n number of inputs and one output, whenever a bit is effaced, total (n-1) bit of data will be destroyed which cannot be recuperated and hence, will result in garbage bits. So, for the reduction in such garbage bits here we will use the concept of reversible gates which means once the input values are supplied to the system, inputs bits can be regained back and hence bit loss can be prevented along with heat loss and ultimately power dissipation can be reduced to the maximum possible extent. The different enhancement parametric quantities for its combination are mentioned underneath:

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1. There ought to be least number of gates utilized.
2. Steady data sources i.e. inputs should be least in number in any reversible logic based system.
3. Garbage outputs i.e. Bit loss has to be least in count.
4. The delay of circuit should be less.

## II. RESTRAINTS FOR REVERSIBLE SYSTEM

A Reversible gate can be taken as an elementary part of digital circuit's that is capable to reduce garbage values with recuperative inputs from logical system. It has following restrictions:

1. The output is supposed to be applied only once which concludes to that it is not allowed to take fan outs
2. A system should be open-chain and hence, has to be an open loop system..
3. All the input vectors are ought be equivalent in number of output vectors for any reversible logic based system
4. All of the input vectors should have singular output vector.

## III. BASIC REVERSIBLE GATES

### *A. FG - Feynman Gate*

FG's are one among the long-familiar reversible gates having two information sources and two output sources with its symbol is given as follows in Fig. 1 along with its input – output combination relation:

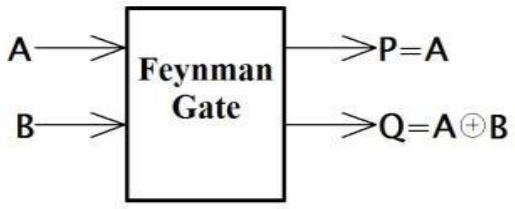


Fig. 1: FG Symbol [10]

### *B. F2G - Feynman Double Gate*

F2G is a (3x3) gate having three information (input) sources and three output sources. The input values are represented as I (A,B,C) and outputs as O (P,Q,R). Also, its relation is shown below in Fig. 2:

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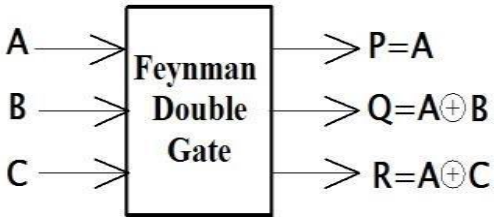


Fig. 2: F2G Symbol [10]

*C. TG - Toffoli Gate*

TG is an invention of Tommaso Toffoli. It can act as universal gate which is also called as CCNOT i.e. controlled-controlled NOT gate and is shown in Fig. 3 along with its 3 inputs and 3 outputs i.e, I (A,B,C) and O (P,Q,R) respectively. Following is the given relational combination of inputs – outputs values.

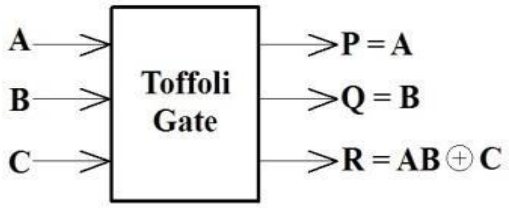


Fig. 3: TG Symbol [10]

*D. FRG - Fredkin Gate*

This Fredkin Gate has three information sources i.e. I (A,B,C) and three outputs sources i.e. O (P,Q,R) depicted in Fig. 4. Input – Output values relations are pictured below:

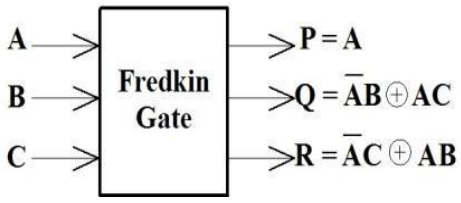


Fig. 4: Fredkin Gate Symbol [10]

This gate has the ability to transmit the first bit invariantly and switches the last 2 bits if 1 is given to first bit.

*E. DKG Gate*

In Fig. 5, a picture of DKG gate is presented which has 4 information (input) sources i.e. I (A, B, C) and four output sources as O (P, Q, R and S). The Boolean expression with rest to input and output

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relation is given below:

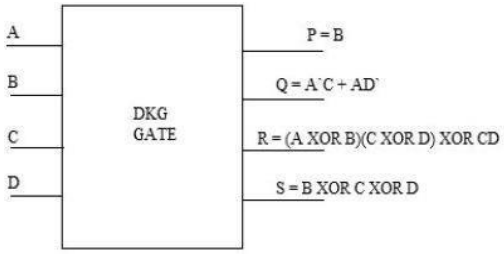


Fig. 5: DKG Gate Symbol [10]

## IV. APPROACHES FOR IMPLEMENTATION OF REVERSIBLE GATES BASED FULL ADDER

### *A. DKG Gate based Full Adder*

Here, a full Adder Architecture has been constructed based on one of the reversible gate's i.e. DKG Gate. DKG Gate's symbol has already been discussed in aforementioned section in Fig. 5 along with all the input and output combinations which shows how the inputs and outputs are mapped. On the grounds of that, a figure of full adder based on DKG gate is presented in Fig. 6 where, the main outputs of a full adder are gathered from R terminal i.e. Carry output and S terminal i.e. Sum output. The rest of the two remaining output terminals i.e. P and Q are depicting garbage values.

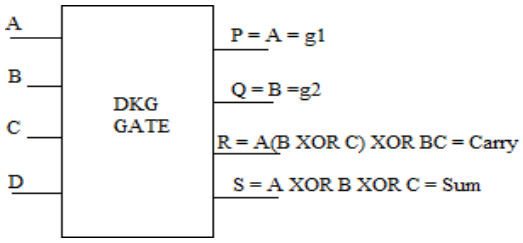


Fig. 6: DKG Gate based Full Adder [10]

### *B. Full Adder using BKG Gate*

Here in this section, another structure is given for full adder designed on the basis of BKG reversible gate. The following figure's i.e. Fig.7 presents symbol of BKG and Fig. 8 represents the input and output terminals along with their input - output mapping. It is shown that just by assigning one of the inputs i.e. D as 0, this BKG gate gives a direct full adder based output at R and S terminal for sum and carry outputs respectively:

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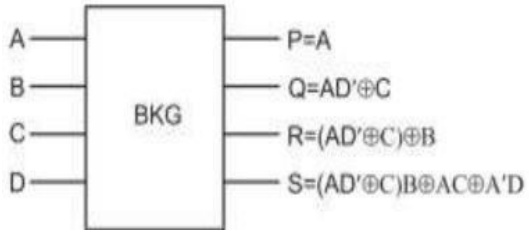


Fig. 7: BKG Gate Symbol [10]

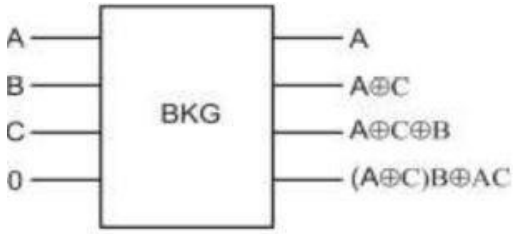


Fig. 8: BKG gate based Full Adder [`10]

*C. Parity Conserving Toffoli Gate based Full Adder*

In this section, first of all, we have mentioned PCTG's symbol in Fig. 9. In the given symbol of PCTG [1] comprises of 4 input sources among which one is taken as invariant value set at 0 and three elementary outputs at the output terminal with one additional garbage. Secondly, the internal circuit of PCTG as depicted in Fig. 10 contains one Feynman double gate and one Fredkin gate. And the final part shows the full adder architecture where, 2 of the Parity Conserving Toffoli Gates's are taken in circuit with each of them conjugated with 2 Feynman double gates as indicated in Fig. 11:

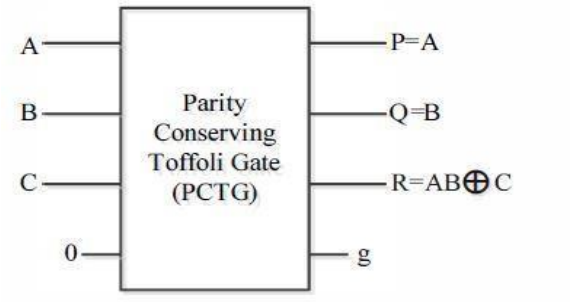


Fig. 9: PCTG Gate Symbol [10]

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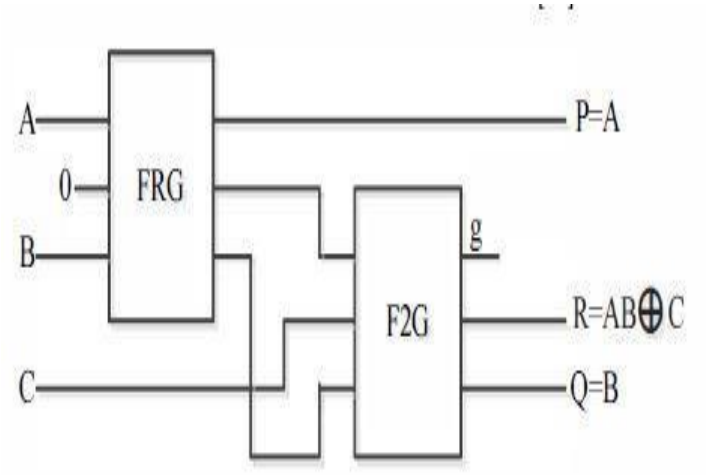


Fig. 10: interior of PCTG [10]

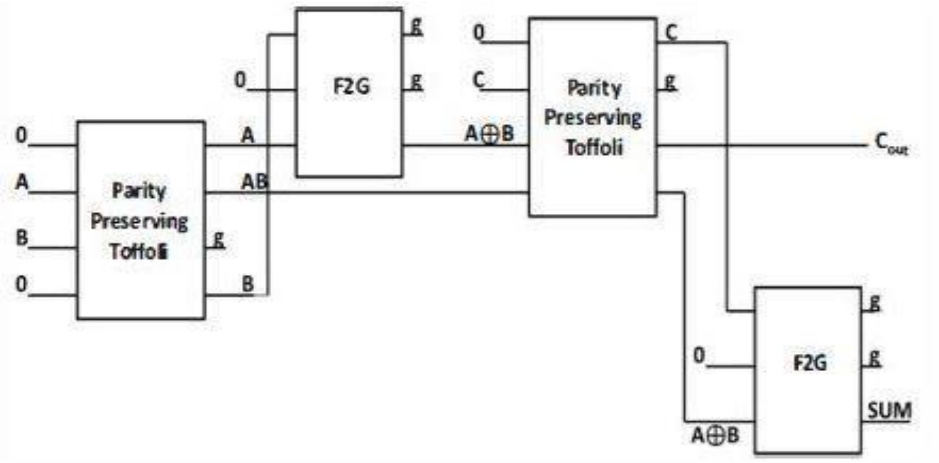


Fig 11: PCTG based Full Adder [10]

## V. RESULTS AND DISCUSSIONS

The Chart 1 i.e. Fig. 12 illustrates the carried out analysis for LP for several Full Adder circuits based on reversible logic at 45nm and 90nm in both the libraries as displayed below:

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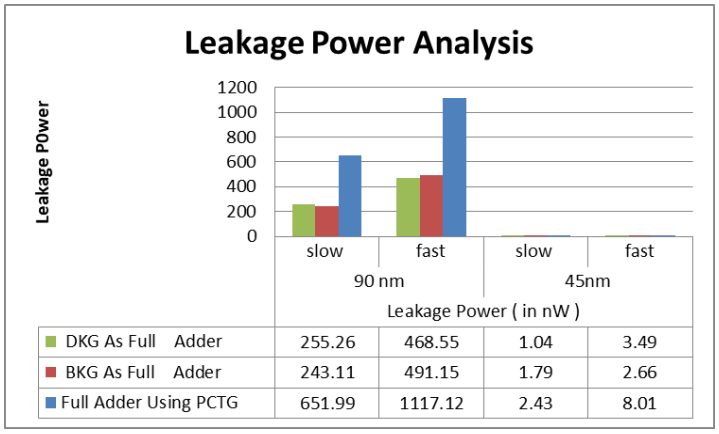
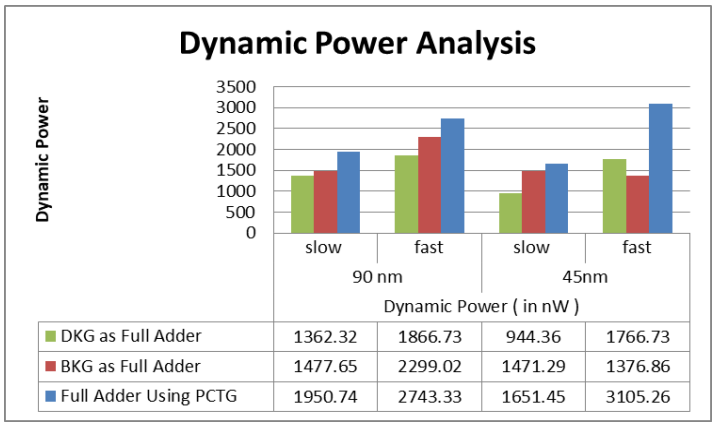



| | | | | |
|---|---|---|---|---|
| DKG As Full Adder | 255.26 | 468.55 | 1.04 | 3.49 |
| BKG As Full Adder | 243.11 | 491.15 | 1.79 | 2.66 |
| Full Adder Using PCTG | 651.99 | 1117.12 | 2.43 | 8.01 |

Fig. 12: Performance evaluation of LP ( Leakage Power)

The Chart 2 i.e. Fig. 13 represents the carried out analysis w.r.t. DP of the different architectures of Full Adder based on reversible logic at 45nm and 90nm in both the libraries as represented below:




| | | | | |
|---|---|---|---|---|
| DKG as Full Adder | 1362.32 | 1866.73 | 944.36 | 1766.73 |
| BKG as Full Adder | 1477.65 | 2299.02 | 1471.29 | 1376.86 |
| Full Adder Using PCTG | 1950.74 | 2743.33 | 1651.45 | 3105.26 |

Fig. 13: Performance evaluation of DP (Dynamic Power)

The following Chart 3 i.e. Fig. 14 illustrates the carried out analysis of Delay of the several architectures of Full Adder based on reversible logic at 45nm and 90nm in both the libraries as shown below:

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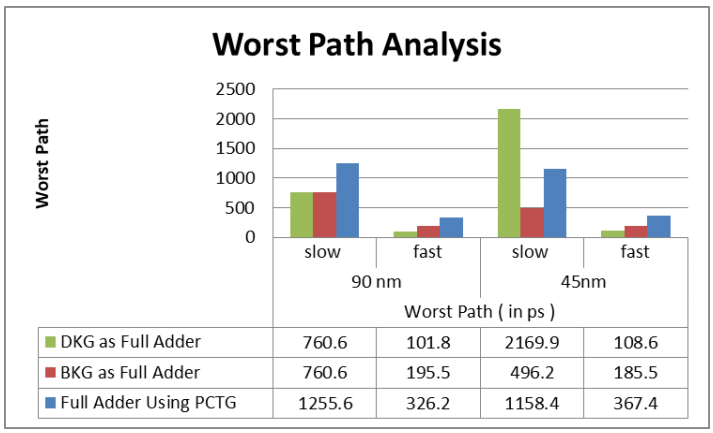
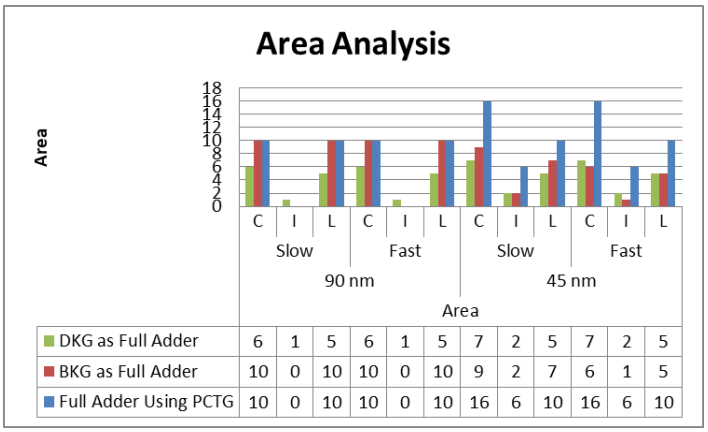



| | | | | |
|---|---|---|---|---|
| DKG as Full Adder | 760.6 | 101.8 | 2169.9 | 108.6 |
| BKG as Full Adder | 760.6 | 195.5 | 496.2 | 185.5 |
| Full Adder Using PCTG | 1255.6 | 326.2 | 1158.4 | 367.4 |

Fig. 14: Performance evaluation of Delay (Worst Path)

The following Chart 4 i.e. Fig. 15 illustrates the Area analysis of the several circuits of Full Adder based on reversible logic at 45nm and 90nm in both the libraries as follows:




| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DKG as Full Adder | 6 | 1 | 5 | 6 | 1 | 5 | 7 | 2 | 5 | 7 | 2 | 5 |
| BKG as Full Adder | 10 | 0 | 10 | 10 | 0 | 10 | 9 | 2 | 7 | 6 | 1 | 5 |
| Full Adder Using PCTG | 10 | 0 | 10 | 10 | 0 | 10 | 16 | 6 | 10 | 16 | 6 | 10 |

Fig. 15: Performance evaluation of Area

## VI. CONCLUSION

The outcomes have demonstrated that full adder utilizing DKG Gate is exhibited to be the best decision as it has most reduced DP at 90 nm technology though Full adder utilizing BKG Gate has least LP and has its industriousness where user's significant concern is power. In addition with that, most noticeable least delay provided and consumes lesser area in comparison with both the full adders' structures in 90nm technology. So, DKG Gate based full adder proves to be the best architecture in terms of all three aspects i.e. Power, Speed and Area at 90 nm technology. At 45 nanometer technology in slow library, Full adder utilizing DKG gate outperforms whereas in fast library, BKG is predominant in execution as far as both DP and LP is concerned. Full adder employing BKG has least Delay in slow library and on contrary, Full adder employing DKG has lowest Delay in fast library among all. Along with that, Full Adder utilizing DKG gate also has smallest area and is considered to be most area efficient in both slow

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and fast libraries.

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