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Reduction of short channel effects in Metal Oxide Semiconductor Field Effect Transistors: A Literature Review

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Abstract-

CMOS is used as major switching element in most of the VLSI circuits but its performance is limited by short channel effects due to scaling of FETs like higher subthreshold (SS), reduced I_{on}/I_{off}, drain induced barrier lowering (DIBL), surface scattering etc. which hampers the performance in nanometer regime. Researchers are now looking for the possibility to choose an alternative device with better electronic and mechanical properties, compact size and lesser power consumption. Going from bigger transistors to smaller ones, these short channel effects come into picture. To settle the tradeoff between these two things, different channel alternatives are being introduced like Carbon Nano Tube FET, Carbon Nano Wire FET, Tunnel FET, Ferroelectric FET and Negative Capacitance FET and many more. Scope is to reduce short channel effects by choosing an ultra-thin body and operate the device under sub-60 mV/decade to reduce power consumption. This paper explains different alternatives of MOSFETs and their control over various parameters to enhance the performance and scaling of FETs.

Keywords- *Subthreshold Swing, Carbon Nanotube FET, Tunnel Field Effect Transistor, Nanowire Field Effect Transistor, Negative capacitance FET.*

1. Introduction

With the advancement in technology and new insights of MOSFET fabrications, power consumption in VLSI circuits has been optimized to a greater extent. However, with the increase in density and compactness of transistors, subthreshold swing (SS) becomes higher than (60mV/dec) and leakage current also increases for a constant I_{on} [3,8]. MOS transistor have been scaled to nanometer feature size so as to make it compact and power efficient. According to Moore's law, silicon-based technology has grown so much and has facilitated the fabrication of power efficient yet faster devices. But, nowadays MOSFET is approaching towards the lower limit in context to feature size [3]. Shrinking the length of MOSFETs gate in nanometer regime, introduces several critical issues and reliability problems such as reduced channel control, introduction of short channel effects, more leakage current and more-power consumption etc. [3]. The most common trend for lowering

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power consumed by VLSI circuits is to alter the supply voltage. But after the specific value, the threshold voltage of MOSFET hinders the further lowering of supply voltage [3]. The threshold voltage of MOSFET used in designing of circuit is the lower limit, voltage supplied must at least be equal to or greater than the threshold.

While reducing feature size of transistors, various unwanted problems have introduced, these are referred as short channel effects like higher subthreshold (SS), reduced I_{on}/I_{off}, drain induced barrier lowering, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Carrier Injection are some of the short channel effects that increases the leakage current and makes SS higher. With the intervention of these effects, MOSFET starts behaving differently and it impacts the performance. The researchers are working towards finding an alternative device in nanometer regime to replace the conventional MOSFET without compromising on performance and overcome the limitations of MOSFET.

Rest of the paper is organized in four sections. Section 2 briefs about the alternative devices available in nanometer regime, Section 3 illustrates the concept of negative capacitance and performance comparison of negative capacitance devices. Lastly, Section 4, concludes the review done and provides the optimal solution to overcome the short channel effects and other constraints of scaling.

2. MOSFET and its Alternatives

With day by day scaling of MOSFET, traditional semiconductor devices have led researchers to look into other alternative devices like Carbon Nanotube Field Effect Transistor (CNTFETs), Carbon Nano Wire Field Effect Transistor, Tunnel Field Effect Transistor, etc. [4,9]. These devices play a very vital role to overcome the problems associated with MOSFET in nanometer regime, with arising short channel effects (due to scaling).

2.1 Carbon Nano Tube Field Effect Transistor (CNTFET)

The term carbon nanotube originated from a Latin word “carbo”, being driven from a French word “charbon” which means charcoal [5]. CNTs are cylindrical in shape, having an extraordinary strength and good electrical properties. Depending on their chirality, they can act as conducting, insulating or semiconducting [5,9]. CNTs are made up of thick sheets of carbon forming long hollow structure to act as channel.

2.1.1 Classification of Carbon Nanotubes:

Classification of Carbon Nanotubes can be done based on chirality, conductivity and number of layers.

Depending upon number of layers, CNTs can be classified as:

(a) Single Walled;

(b) Multi Walled;

(c) Mixed Walled.

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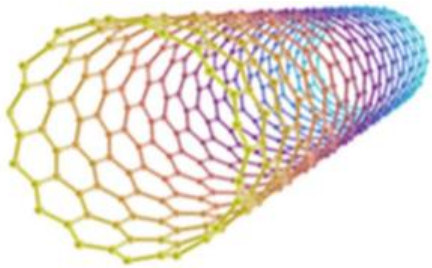

Figure 1: Single Walled Nano Tube (SWNT)

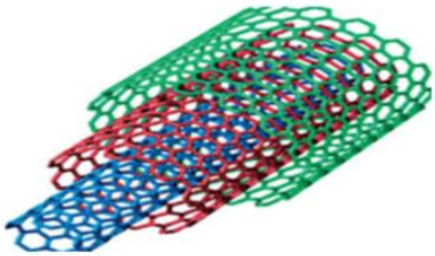

Figure 2: Multi Walled Nano Tube (MWNT)

Depending upon chirality, CNTs can be classified as:

(a) Armchair;

(b) ZigZag;

(c) Chiral.

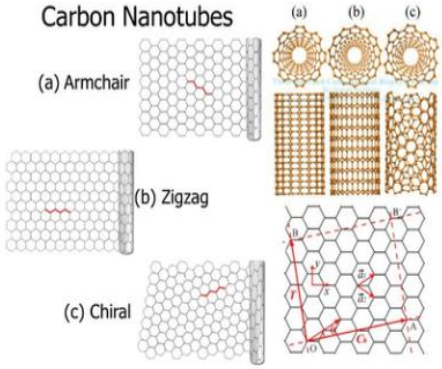

Figure 3: Structure of Carbon Nanotube a) Armchair b) ZigZag c) Chiral

Carbon nanotube field-effect transistors have been fabricated on the structure of MOSFET only. It has similar three terminals namely source, gate and drain. Among these, Gate plays the most vital role of controlling the current flow across source and drain. Silicon (Si) channel of MOSFET is replaced by Carbon nanotube in CNTFET and the switching of gate i.e. turning on and turning off controls the current to flow through CNT channel [5].

2.2 Nano Wire Field Effect Transistor

Single-silicon nanowire field-effect transistor (SiNW-FET) devices are popular these days for their quantification and powerful detection of biochemical molecules. First reported in 2001, SiNW-based biosensors are of very compact size but they were highly sensitive in detection of various chemicals and biological species in real-time. However, conventional SiNW-FET sensors exhibit low voltage outputs due to high intervention of noise, that results from the electrical property deterioration caused by the dry etching process and are very lesser in magnitude [6]. Application based, (SiNW)-based sensors have a great potential for doing biochemical analyses [6].

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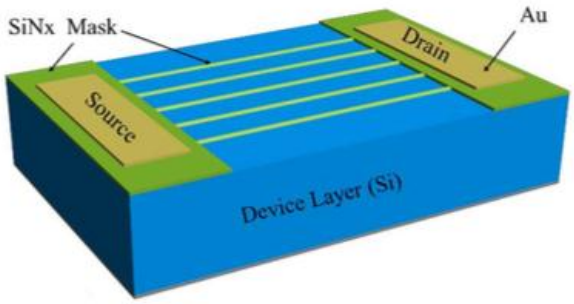

Figure 4: Nanowire FET (NWFET)

2.3 Tunnel Field Effect Transistor

Tunnel field-effect transistor (TFET) is promising solution for replacing MOSFET as a switch for future logic implementations. However, due to lack of tools available for device fabrication and design constraints of moderate tunnel junction, TFET are face challenges in making the subthreshold slope (SS) steeper, which is directly associated with the power consumption, and channel control. In tunnel FETs band-to-band tunneling of carriers acts as a major carrier injection phenomenon across reverse biased PN junction. There are three major benefits of this injection mechanism: 1) Truncation of high energy fermi-tail 2) due to reverse bias operation, low off state current 3) I_{ON} is dependent upon tunneling width and area i.e. tunneling parameters. This removes the constraint of lowering subthreshold slope below 60 mV/decade and results in reduction of leakage current and scaling of threshold voltage [10]. Inspite of above listed benefits, there are certain drawbacks like low I_{ON} and higher SS, which hinders the replacement of conventional MOSFET with tunnel FET in low power circuits [7]. To overcome these drawbacks, Tunnel FET is fabricated in different topologies depending upon gate electric field (Vg) and tunneling junction electric field. Following two topologies are famous in TFET:

- Lateral Tunnel Field Effect Transistor (LTFET);
- Vertical Tunnel Field Effect Transistor (VTFET).

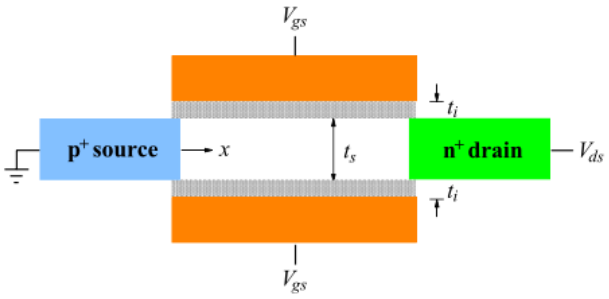

Figure 5: Tunnel FET (TFET)

3. Concept of Negative Capacitance in FETs

Negative capacitance (NC) FETs fabricated using Hafnium-based ferroelectric material stacked with a conventional MOSFET (MFMIS structure) overcomes the physical limitation and possesses a steeper sub-V_{TH}

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swing (SS) lesser than the physical limitation (60 mV/decade). Due to this reason, negative capacitance transistor has been considered for usage in lower power VLSI circuits in recent years [8]. First reported in 2007 by Giovanni et. al. [1], Negative capacitance associated with Fe layer is the main factor of low SS swing in Fe-FET transistors. Moreover, it provides high I_{on}/I_{off} and ample voltage amplification; with particular selection of ferroelectric material to form gate stack [1]. By incorporating a thin layer of ferroelectric material with High-k dielectric for making gate stack (Inspite of gate of a standard MOSFET), it is feasible to overcome the physical subthreshold limit (i.e. 60mV/decade) at room temperature [1,11].

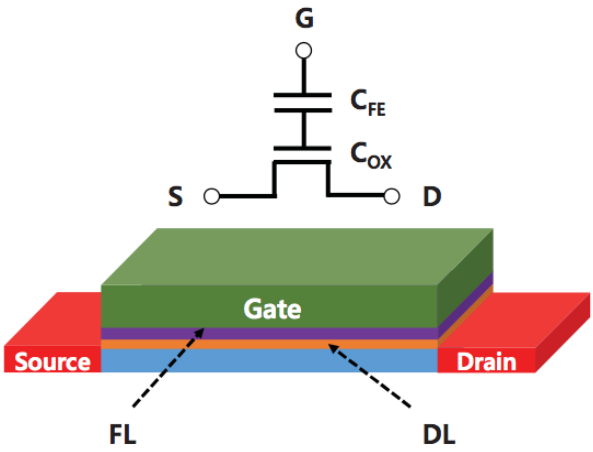

Figure 6: Negative Capacitance FET (NCFET)

In above figure, Ferroelectric material is adopted as the Ferroelectric layer FL which brings Negative capacitance effect on gate dielectric layer (DL). Negative Capacitance devices can become one of the most promising alternatives with steep SS slope and can be used for low-power logic circuit applications [12].

3.1 Effect of Negative Capacitance in FETs

Negative capacitance has been tried on various MOSFET alternative and following results have been obtained in context of SS and Ion/Ioff.

Table I. SS and Ion/Ioff comparison of various NCFETs

Device	SS (mV/dec)	I_{on}/I_{off}
NC-TFET	44	10^9
NC-NWFET	43.85	10^8
NC-CNTFET	55	10^{10}

It has been observed that the lowest SS is achieved in case of bi-layer stacked nanowire gate-all-around (GAA) negative capacitance (NC) field-effect transistors (FETs). In (NW-GAA-NC-FET) a metal-ferroelectric-metal-insulator-semiconductor (MFMIS) stack is used [16]. This can be further extended to get a steeper SS swing

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with optimal selection of Fe and High-k materials without compromising much on performance. On the other hand, NC-Carbon nanotube provides highest I_{on}/I_{off} at a constant I_{on}. The following graph shows the effect of negative capacitance on subthreshold swing of various FET devices [15,16,20]. SS is an important parameter. It has been seen that the design and fabrication of these negative capacitance devices have subsequently reduced the SS swing < 60 mV/decade thus facilitating better channel control and lesser power consumption.

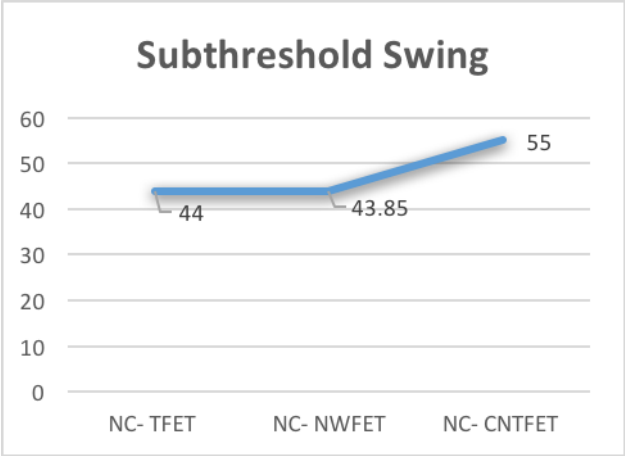

Figure 7: SS swing comparison of different Negative Capacitance MOSFETs

4. Conclusion

The use of negative capacitance phenomenon in FETs enables the possibility of having a sub- subthreshold swing lower than 60 mV/decade without comprising on current ratio and to exhibit lower current leakage. Theoretically, Conventional CMOSs exhibits a subthreshold swing as low as about 60 mV/decade at room temperature. With smaller subthreshold swing, channel control will also become better, e.g. improved I_{on}/I_{off}, which usually reduces the current leakage and power consumption. For optimizing VLSI circuits, all these factors leads to a better performance. Therefore, Negative capacitance FETs could be a worthwhile alternative to the conventional MOSFETs.

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