ISSN:0971-1260
Vol-22-Issue-37-December -2019

Performance Analysis of Double Gated $In_{0.53}Ga_{0.47}As$ Heterojunction TunnelFET for Low Power Applications

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ABSTRACT

With continuous scaling in MOSFETs, short channel parameters are putting a serious stumbling block on the miniaturization. In that regard, Tunnel FETs are seen as a promising device to provide a solution to this issue. TFETs work on the basis of band to band tunneling, and has the ability to provide high I_{ON}/I_{OFF} ratio, and a steeper subthreshold slope. However, using a conventional silicon as a material deter the performance of TFETs because of larger energy band gap of a silicon as a result tunneling phenomenon is suppressed. In this paper, we present a solution in the form of Group III-V based semiconductors, which are direct band gap materials rather than a silicon, which is an indirect bandgap material. Moreover, it has been established by the results that a double gated TFETs perform better because of the greater controllability provided by the gate over the channel.The ON OFF currents of a device are 0.1µA/µm and 10 fA/µm, with I_{ON}/I_{OFF} ratio of around 10^7. The subthreshold swing at lower drain voltages is around 54 mV/decade, which is better than the ideal value achievable in the MOSFETs.

Keywords:*TFET, MOSFET, band to band tunneling, subthreshold swing, III-V Semiconductors*

1. INTRODUCTION

Electronics has undergone several changes over last forty years starting from bulky vacuum tubes to lighter and low cost bipolar junction transistors to unipolar field effect transistors (FETs) and currently CMOS (complementary metal oxide semiconductor) technology. The reason that one technology was superseded by the other was when their power consumption became excessively high [1]. Several challenges like short channel effects have made it difficult to allow continuous miniaturization due to CMOS scaling. Therefore, the need arises to explore new emerging devices that can improve the limitations of CMOS technology and can be seen a future prospect and successor of conventional MOSFET [2-5].

Diodes based on tunneling phenomenon were reported earlier by Richard et al [6]. The limitation in a single gated TEFT was the low ON current and the poor subthreshold swing. Boucart et al first introduced a double gated TFET design based on high-K dielectric materials[7]. However the use of a silicon limits the I_{ON} of the devices. To increase the I_{ON} further with a steeper subthreshold swing, researchers have explored new materials. Group III-V TFETs are being studied to solve low ON drive currents of a device.Various techniques have been used by researchers for the fabrication of GaAs interface [8, 9]. $Si_{1-x}Ge_x$ have also been utilized as a material for the design process, however more molar presence of Si in it increases the tunneling width which is not desired[10]. InGaAs introduced by Mokherjee et al, achieved subthreshold

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

swing of 250 mV/decade[11]. This was further improved by Zhao et al, improved subthreshold swing of 90 mV/decade [12]. This paper has achieved steeper subthreshold swing and will be useful for low power applications.

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

2. GROUP III-V SEMICONDUCTORS

These are the materials obtained by combining group III elements of a periodic table (aluminum, indium and gallium) with group V elements of a periodic table (nitrogen, phosphorus, antimony and arsenic). The atoms in III-V compound semiconductors have covalent bonds similar to the group IV elements like silicon. The binary III-V compounds can be further mixed together to obtain ternary and quaternary compounds. The binary compounds $A^{III}C^{V}$ and $B^{III}C^{V}$ can be combined in the ratio to obtain a ternary compound A^{III} x B^{III} (1-x) C^{V}. The properties of A^{III} x B^{III} (1-x) C^{V}lies in between of $A^{III}C^{V}$ and $B^{III}C^{V}$and can be varied from 0 to 1 by varying its molar fraction.Some of the popularly investigated compounds used by researchers are: GaAs, InGaAs, GaSb, InAsSb, InAlAs, etc. The tunneling rate in III-V semiconductors are higher because of its smaller band gap, smaller tunneling mass and direct tunneling mechanism in contrast to indirect tunneling mechanism of silicon. However, again due to their smaller band gap, I_{ON} and I_{OFF} both become high in TFETs. Furthermore, in order to increase I_{ON} and reduce subthreshold swing band engineering to increase band to band tunneling has been employed[13].The selection of the InGaAs as a material is based on its lower energy band gap, variation of band energy as per the molar fraction being chosen and the tuning of lattice matching with broader range of alloy compositions.

3. DEVICE STRUCTURE

In this paper, we have implemented a TFET structure based on a group III-V semiconductor $In_xGa_{1-x}As$ with mole fraction x = 0.47. Since its energy band gap is lesser (Eg=0.85 eV) than that of a silicon (E_g=1.1 eV), so tunneling phenomenon increases due to the lesser tunnel width. Visual TCAD software has been used to perform the simulation. The local tunneling based on drift-diffusion mechanism has been used to produce results. Moreover, Kane's Model for band to band tunneling has been used, and can be expressed as:

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}.\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right)(1)$$

Where E represents the magnitude of an electric field, E_g is the energy band gap of the material. While as. A.BTBT and B.BTBT are the empirical fitting parameters [14]. From equation (1), it is clear that the tunneling efficiency of band to band tunneling is highly dependent on the energy band gap of the material.Materials with a smaller and direct bandgap could greatly increase the band-to-band generation rate and thus increase the ON current of TFETs.

The gate voltage is a crucial part in determining the performance of TFETs. Thus, to increase the control over the channel, double gated structure has been preferred instead of a single gate structure. This will lead to higher ON current as well. In the given structure, as shown in Figure 1.In this, Source region is highly doped with p-type, drain region is highly doped with n-typeand channel region is moderately doped with p-type. N-polysilicon is used for gate and HfO_2 high-k dielectric is used as the gatedielectric. Aluminum contacts are used for source and drain regions. The meshing is heavier at the gate-source junction region to enhance tunneling, as illustrated in Figure 2.The parameters used for the device has been summarized in table I.

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

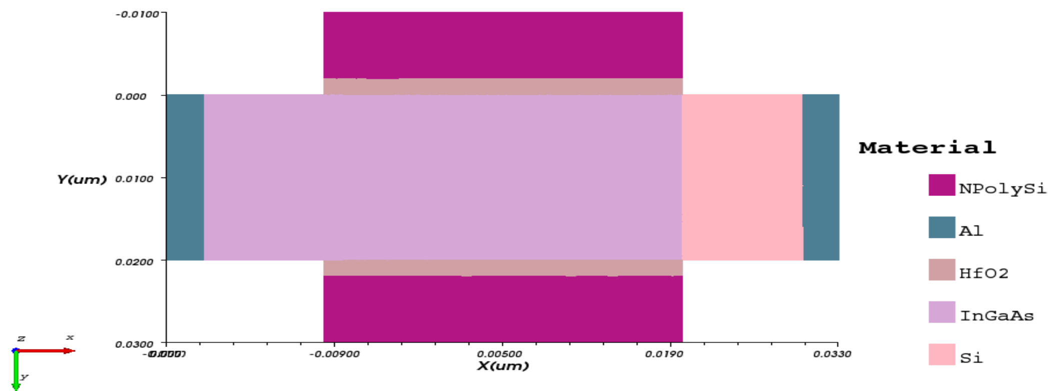

Figure 1: Double Gated InGaAs Heterojunction structure

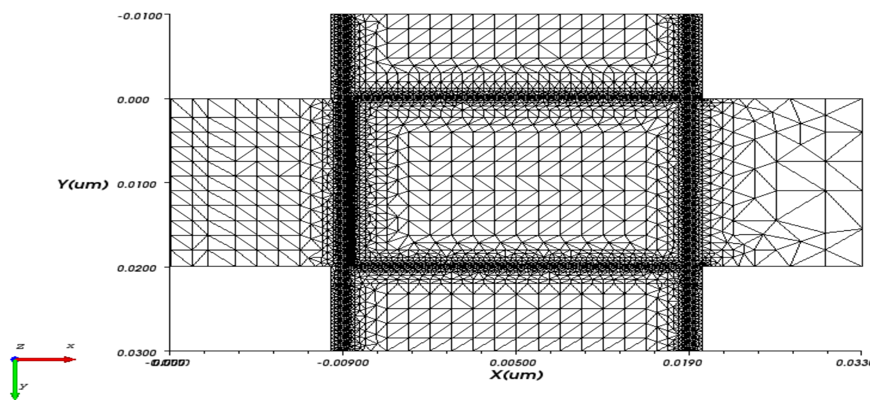

Figure 2: Meshing structure for double gated InGaAs Heterojunction structure

TABLE I:

Parameter	Values
Gate Length	30 nm
Source doping	$1x10^{20}$ cm^{-3} (p-type)
Channel doping	$1x10^{16}$ cm^{-3} (p-type)
Drain doping	$5x10^{18}$ cm^{-3} (n-type)
Oxide Thickness	2 nm
Gate Workfunction	4.7 eV

4. RESULTS AND DISCUSSIONS

The energy band diagram for various gate-source voltages are provided in Figure 3. It is clear that the tunneling width deceases as the gate to source voltage is increased, hence providing a way for band to band tunneling with electrons shifting from the valence band towards the conduction band.The drain current response to the applied gate voltage has been illustrated in Figure 4. The gate voltage has been swept from o volts to 2 volts with a step size of 0.1 volt, while as drain-source voltage has been kept constant for a particular simulation. It is clear from the curves that the minimum leakage current is obtained at V_{ds}=0.1V, and is therefore suitable for low power applications. It is clear from Figure 4 that $I_{OFF}$for a device is around 10

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

femtoamperes/micrometer, while as the ON current is of the order of 0.1 microamperes at higher drain voltages, with I_{ON}/I_{OFF} ratio of about 10^7.

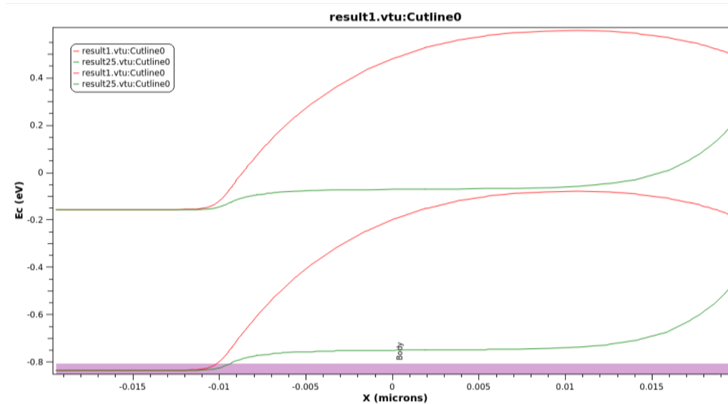

Figure 3: Energy Band Diagramfor double gated InGaAs Heterojunction structure

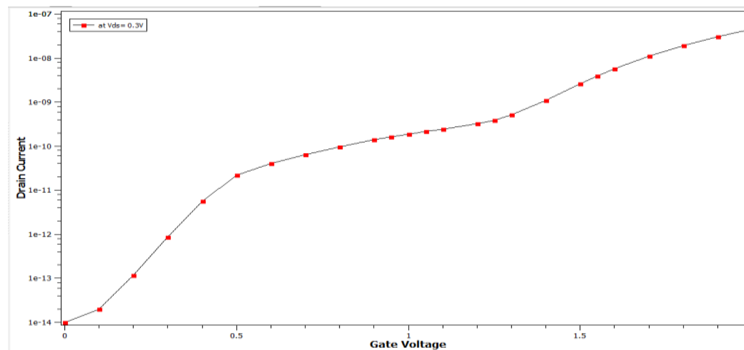

Figure 4: Id-Vgs characteristicsfor double gated InGaAs Heterojunction structure

The amount of gate voltage needed to increase the drain current by 10 folds is called as subthreshold swing and its units are mV/decade. This parameter must be as small as possible so that even a little change in the gate voltage can produce larger change in the drain current, thus making a transistor suitable for low voltage operation.

The expression for the subthreshold region is given by:

$$S = \frac{dV_G}{d\psi_s}\frac{d\psi_s}{d(\log_{10} I_D)} \cong (1+\frac{C_d}{C_{ox}})\ln 10\frac{kT}{q} \qquad (2)$$

Where V_g is the gate voltage,Ψ_s is the surface potential, I_D is the drain current, C_d is the depletion capacitance, C_{ox} is the oxide capacitance and kT/q is the thermal voltage. For a MOSFET the ideal value that can be achieved is 60 mV/decade. At low V_{Ds} operations subthreshold swing for InGaAs based TFET is around 54 mV/decade. However, if the drain voltage is increased, then the average subthreshold swings is around 115 mV/decade.

The distribution of electrons and holes across the device provides an idea regarding the doping levels added at the source, channel and the drain junctions. The distribution would be higher as gate voltage would increase. The electrical potential variation from Vgs= 0 volts and Vgs= 2

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

volts have been analyzed. Finally, we have compared the power consumption of single and double gated InGaAs Heterojunction structure. Figure 5 shows the illustration of these parameters.

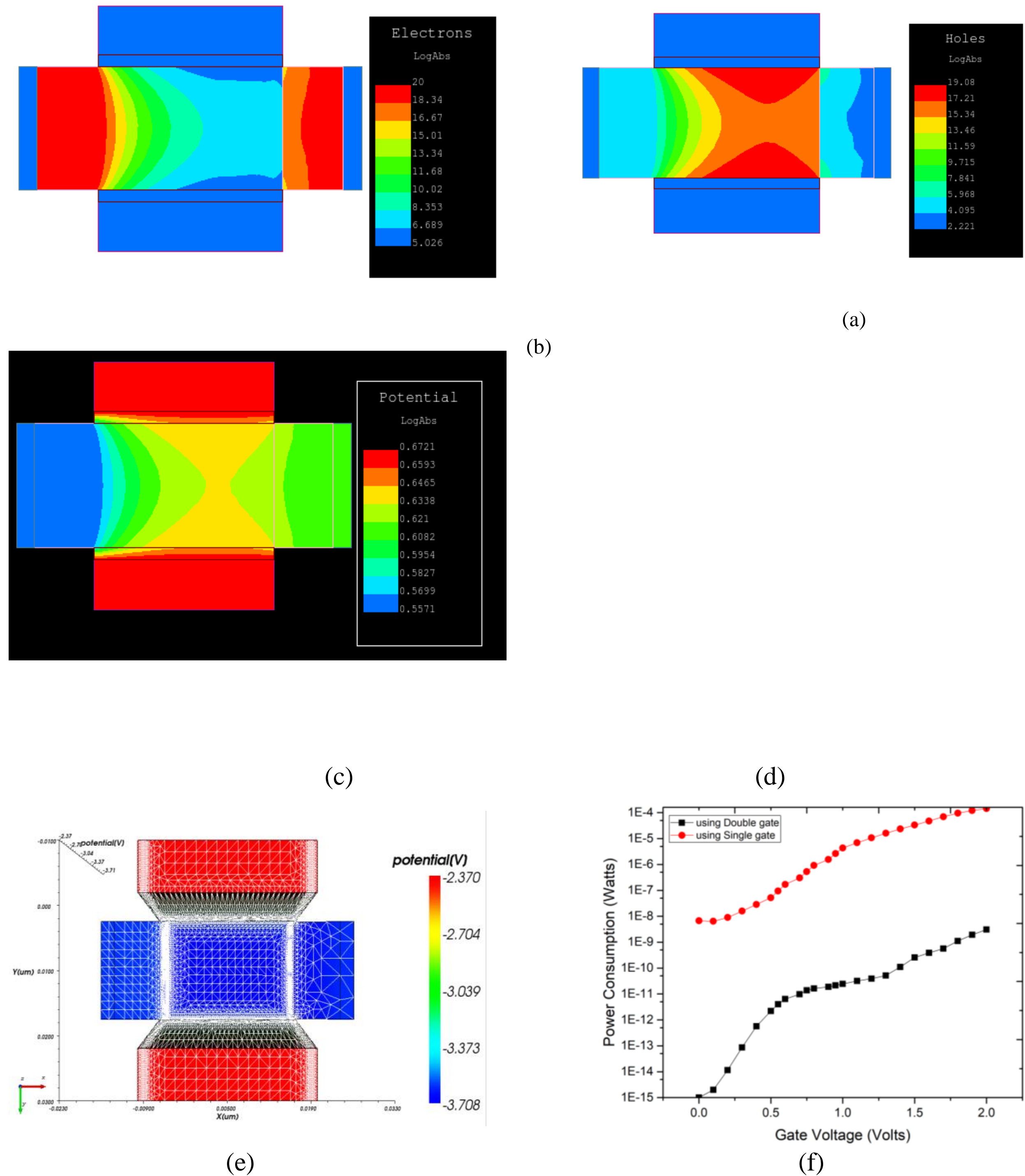

Figure 5: (a) Electron distribution (b) Hole distribution (c)Potential variation (d) Potential at Vgs= 0 volts (e) Potential at Vgs=2 Volts (f) Power consumption comparison for a single and double gate InGaAs Heterojunction structure

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

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ISSN:0971-1260
Vol-22-Issue-37-December -2019

5. CONCLUSION

The continuous miniaturization of ICs due to the scaling faces a major hurdle due to the short channel effects. So, the need of an hour is to come up with the novel materials that can potentially replace MOSFET technology in future. TFETs are a step towards achieving that goal. Although conventional TFETs suffer from low ON current and higher subthreshold slope.However, this paper has proposed InGaAs based Heterojunction TFET as a device for improving ON current along with a steeper threshold slopes. Moreover, our results reveal that the use of double gate would enhance the ON current due to greater controllability of the gate over the channel. The ON OFF currents of a device are 0.1μA/μm and 10 fA/μm, with I_{ON}/I_{OFF} ratio of around 10^7. The subthreshold swing at lower drain voltages is around 54 mV/decade, which is better than the ideal value achievable in the MOSFETs. Due to the higher ON current and a steeper subthreshold swing, the device may be used for low power applications like RF rectifier designs for RF-powered systems [15] and biosensors [16].

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