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Pull Up and Pull Down Network Base Design of Comparator with Adiabatic Logic

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ABSTRACT

This paper presents the design and analysis of Pure Double Tail Comparator & Pure Dynamic Comparator. The enhancement in energy in Power dissipation, and Delay is one of the major challenging issues in the field of VLSI design model. Therefore, the use of adiabatic logic offer significant Power Dissipation and Delay problem as compare to Pure Double Tail Comparator and Pure Dynamic Comparator. The Double Tail Comparator has been design with adiabatic logic and it is simulated. Partially adiabatic Logic design technique is used in this paper . Analysis is done on the basic of performance parameters, which are compared in the terms of Power Dissipation, and Delay. In this paper, we analyze the performance of Pure Double Tail Comparator (P-DTC) using with Adiabatic Double Tail Comparator (A-DTC) with the variation of frequency (GHz) and temperature (Degree Celsius). Simulation results reveals that the A-DTC is comparatively 90% more power efficient than Pull up and pull down network base design. Further, it also reduces the delay time.

Keywords: Adiabatic Logic, A-DTC, Power Dissipation, Delay Time.

1. INTRODUCTION

The comparator is one of the popular devices, which are used in electronics industry. In analog to Digital Converters (ADCs), comparator requires advanced speed and power efficiency. ADCs extensively used in several applications including fast serial links, datum storage system and advance speed measurement apparatus [1]. The commonly used ADCs are Flash ADC, Successive approximation converter, Sigma delta etc [2]. All these perform variant functions and have its own advantages and disadvantages [3]. Therefore, the functioning of these ADC is significantly relay on the type and several logic circuit used during the formation of these comparator circuit [4]. SAR type ADC comparator control the functioning of ADCs without intrinsic gain, fallacy correction. In ADC, comparator compares the differences between the two analog signals and provides a single output in the digital form [5]. It can be design by using of multiple parts like op-amp, diodes and transistors. Here Op-amp is completely suited for comparator utility because of its advanced input impediment and extensive open loop gain [6]. The comparator has several assiduity such as switching power regulators, data transfer and relaxation oscillator, BLDC operation motor and peak detector etc [7]. Designing of a low power consumption circuit is one of the main challenging issues in the field of VLSI design [8]. The adiabatic is a one of the best-suited technique to mitigate this issue [9]. The adiabatic logic works on charge recovery principle in which energy is re-use again instead of dissipation [10]. The use of adiabatic switching is to diminish energy loss through the charged/discharge cycles [11]. To reduce the power dissipation in adiabatic switching, all the nodes are charge/discharge at steady current [12]. The adiabatic are of two types fully adiabatic and partially adiabatic circuits (quasi-adiabatic circuits) [6]. There are so many adiabatic techniques are available in the literature like Positive Feedback Adiabatic Logic (PFAL), Clocked Adiabatic Logic (CAL), Efficient Charge Recovery Logic (ECRL), to provides energy saving and less power dissipation in the logic circuit [2]. Further, the available research literature reveals that the use of adiabatic logic in P-DTC is less explored to reduce the problem of power dissipation. Therefore, in this paper, we analyze a proposed A-DTC circuit with zero power dissipation and reduction in delay.

The rest of this paper has been organized as follows. Section 2 gives an summary of the design model of low power A-DTC. The simulation results are discussed in section 3 and conclusions are obtain in section 4.

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2. DESIGN MODEL OF ADIABATIC DOUBLE TAIL COMPARATOR CIRCUIT (A-DLC)

In this section, we consider a Double Tail Comparator circuit using with adiabatic logic and block diagram of this circuit is shown in Fig. 1 below:

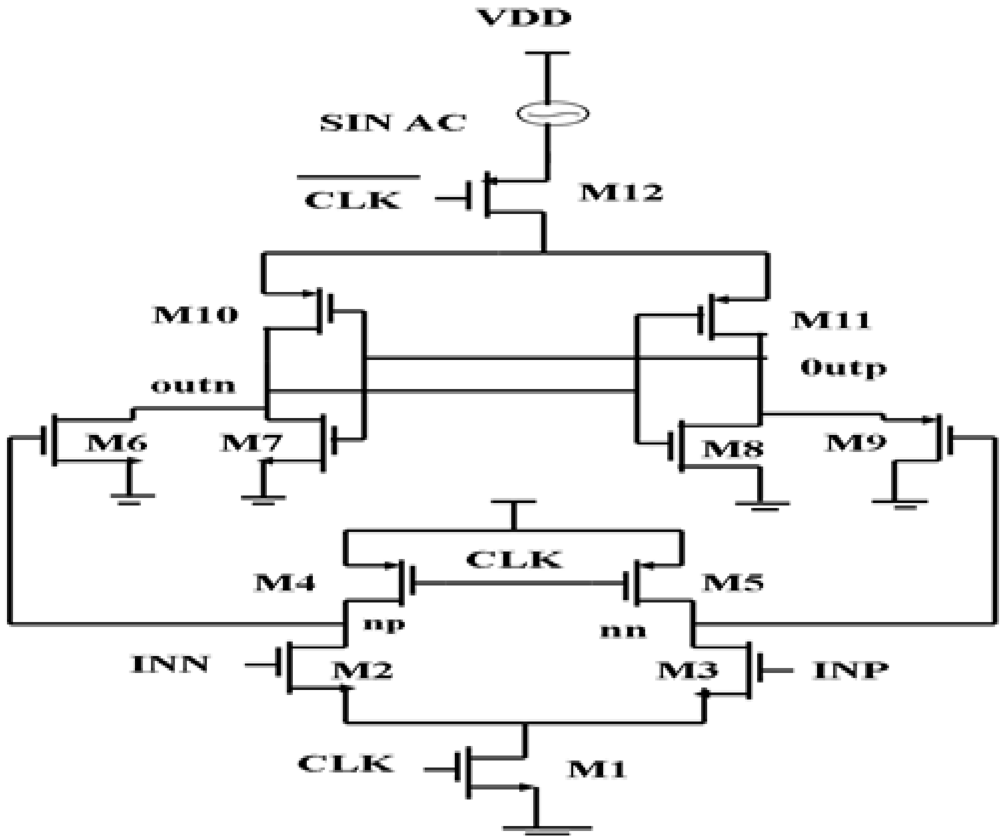

Fig. 1: Proposed Design Model of Adiabatic Double Tail Comparator

In above Fig. 1, When CLK=0, then M1 transistor is off, transistors M4-M5 are used for the logic of pre-charge nn and np nodes to V_{DD}, which in further allow transistor M6 and M9 to discharge path to ground. For the decision-making phase CLK signal is high of value $V_{DD,}$ which allow transistor M1and M2 to conduct on and transistor M4–M5 conduct off; which result in voltage at terminal nn and np to drop according to the function I_{M1}/Cnn(p) and for peak values, differential voltage Vnn(p) will start developing. The comparatively performance analysis of P-DTC, A-DTC, P-DC and A-DC is shown in the next section.

3. RESULTS AND DISCUSSION

In this section, firstly the Power Dissipation (nW) performance of P-DTC, A-DTC, P-DC and A-DC is analyzed with respect to frequency (0 to 4 GHz). The simulation result is shown in Figure 2. Secondly, we analyze the Power Dissipation with respect to Temperature in Fig. 3. In the end, the Vop and Von Delay performance of P-DTC, A-DTC, P-DC and A-DC is analyzed with respect to frequency and temperature, in Fig. 4 and Fig. 5 to Fig. 6 respectively.

3.1. POWER DISSIPATION VERSUS FREQUENCY.

Fig. 2 depicts the comparatively Power Dissipation performance of P-DTC, A-DTC, P-DC, A-DC, analyzed with respect to frequency (0 to 4 GHz). Here, the simulation results reveal that the highest Power Dissipation is observed in the P-DTC. However, the Power Dissipation becomes zero in the A-DTC, P-DC and A-DC. Further, it is also noticed that the Power Dissipation of this comparator is remain almost constant with variation in the Frequency.

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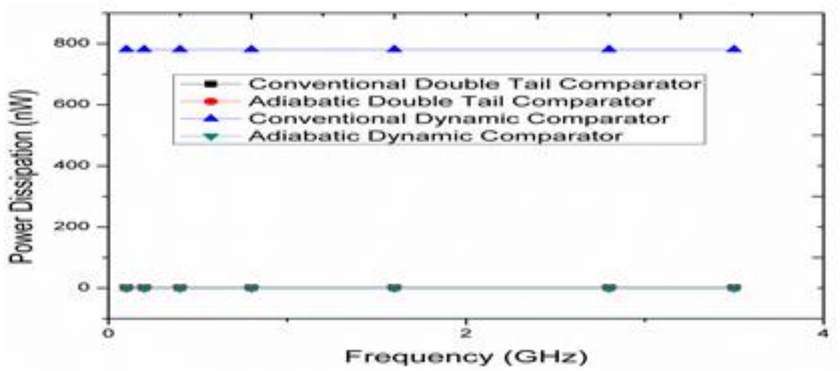

Fig. 2: Power Dissipation (nW) versus Frequency (GHz) of P-DTC, A-DTC, P-DC and A-DC.

3.2. POWER DISSIPATION VERSUS TEMPERATURE.

Here, the Power Dissipation performance of P-DTC, A-DTC, P-DC and A-DC is analyzed with respect to Temperature. In the simulation results, the largest Power Dissipation is observed in P-DC at all temperature. However, it is decreases with increase in the value of temperature. Further, the best performance is observed in both A-DTC and A-DC case. Here, the Power Dissipation is remain almost constant to zero at temperature variation. Therefore, A-DTC and A-DC is more efficient than P-DTC and P-DC.

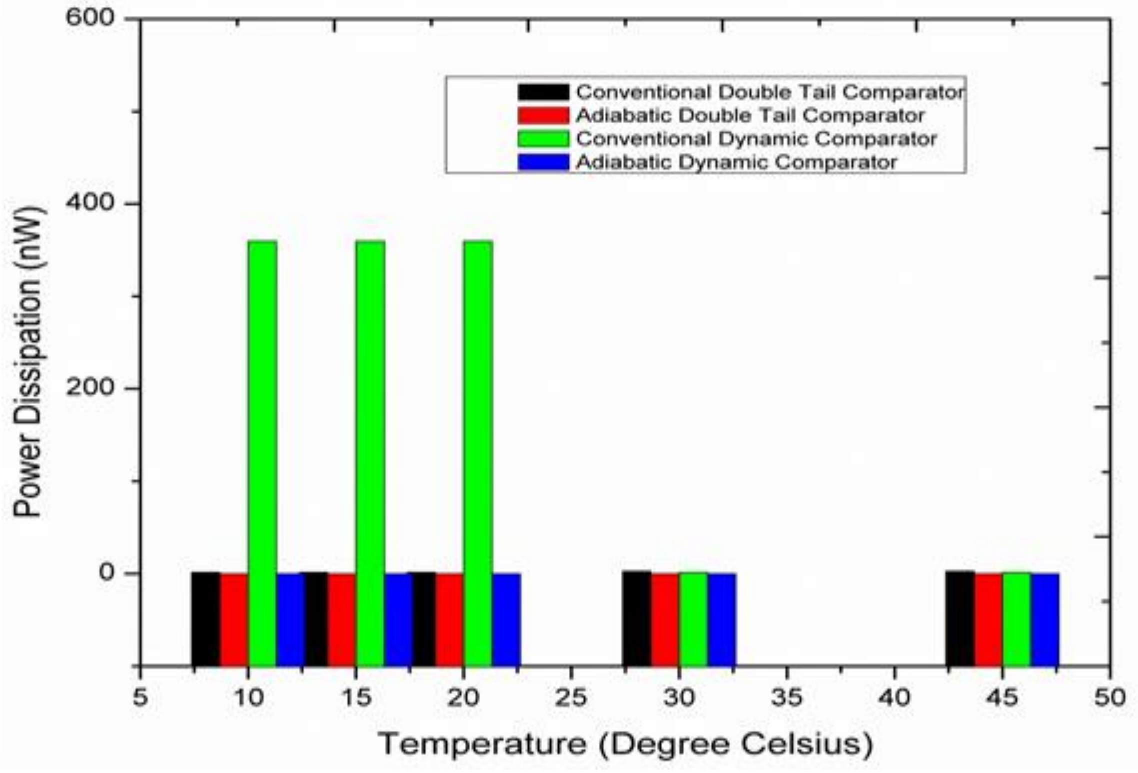

Fig. 4: Power Dissipation (nW) versus Temperature (Degree Celsius) of P-DTC, A-DTC, P-DC and A-DC.

3.3. VOP AND VON DELAY VERSUS FREQUENCY.

Here, the Vop and Von delay performance of P-DTC, A-DTC, P-DC and A-DC is analyzed with respect to frequency. Results in Fig. 5 shows that the both Vop and Von delay decrease with increases in the value of frequency. In addition, the least delay is observed in both A-DTC & A- DC and it reaches up to almost zero at 3.5 GHz frequency. Therefore, it is again concluded that A-DTC and A-DC is more efficient than the P-DTC and P-DC.

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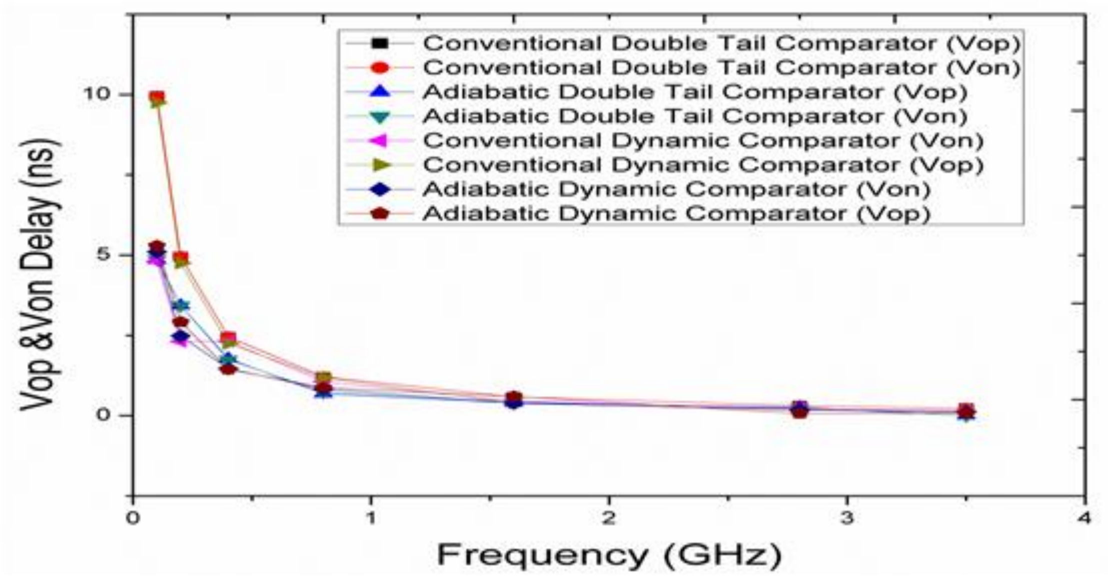

Fig. 5: Vop and Von Delay (ns) versus Frequency (GHz) of P-DTC, A-DTC, P-DC and A-DC.

3.4. Vop and Von Delay versus Temperature.

In Fig. 6 and Fig. 7, we analyze the Vop and Von delay performance of P-DTC, A-DTC, P-DC and A-DC with respect to temperature. Here, both Vop and Von delay remain almost constant with variation in temperature. Further, the least delay is observed in the A-DC. It is also concluded that the delay performance of A-DC is comparatively better than the A-DTC.

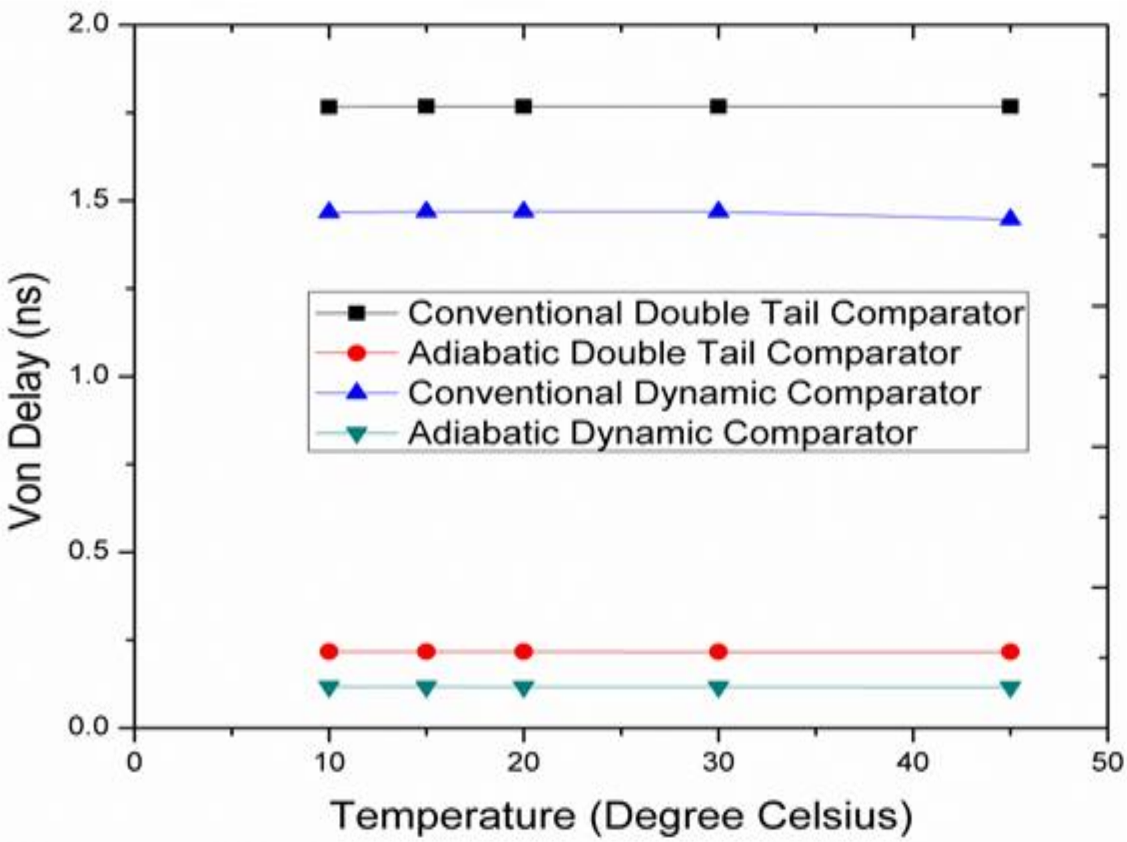

Fig. 6: Von Delay (ns) versus Temperatures (Degree Celsius) of P-DTC, A-DTC, P-DC and A- DC.

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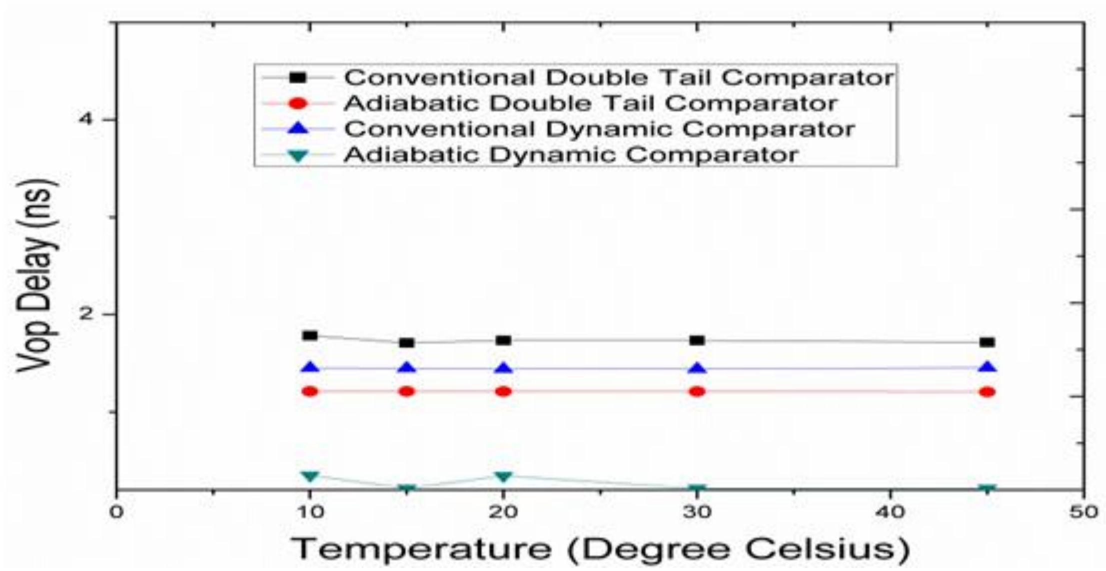

Fig. 7: Vop Delay (ns) versus Temperatures (Degree Celsius) of P-DTC, A-DTC, P-DC and A-DC.

4. CONCLUSION

For reducing Power Dissipation and Delay an alternative partially adiabatic logic design techniques is used. Which reduces the Power Dissipation and Delay as compare to Pure Double Tail Comparator & Pure Dynamic Comparator. It is clearly seen that our main focus is on Power Dissipation and Delay. The Power Dissipation is reduced to zero as compare to PDTC & PDC and the values of delay is also reduced to minimum. So it is clear from the results that Temperature (Degree Celsius) vs. Power Dissipation (nW) & Delay (ns) of Conventional Double Tail Comparator, Adiabatic Double Tail Comparator, Conventional Dynamic Comparator and Adiabatic Dynamic Comparator result is shown which prove that adiabatic circuits is more useful than pure circuits. Reduction in Power Dissipation and Delay in Adiabatic Double Tail Comparator, Adiabatic Dynamic Comparator, is more efficient than Pure Double Tail Comparator & Pure Dynamic Comparator.

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