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Simulation and Design of Low Noise Amplifier

M. Akshaiya
B.E, Electronics and Communication
Sri Sairam Engineering College
Chennai, India
akshaiyamohan@gmail.com

G. Alagulakshmi
B.E, Electronics and Communication
Sri Sairam Engineering College
Chennai, India
alagulakshmigomu@gmail.com

N. Nazeeya Anjum
Assistant Professor
Sri Sairam Engineering College
Chennai, India
nazeeyaanjum.ece@sairam.edu.in

Abstract-A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio. An amplifier increases the power of both the signal and the noise present at its input. A good LNA has a low NF, enough gain to boost the signal and a large enough inter-modulation and compression point to do the work required of it. This paper consists of the LNA designed with ATF-21170 to operate in 2.4 GHz with a gain of 18.267 dB

Keywords-LNA, 2.4 GHz,ATF-21170

I. INTRODUCTION

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio.[8] A good LNA has a low NF, enough gain to boost the signal and a large enough inter-modulation and compression point to do the work required of it. The four important parameters in LNA design are: gain, noise figure and impedance matching

An RF amplifier is an network that increases the amplitude of weak signals. Receiver amplification is distributed between RF and IF stages throughout the system, and an ideal amplifier increases the desired signal amplitude without adding distortion or noise.[1]Unfortunately, amplifiers are known to add noise and distortion to the desired signal. In a receiverchain, the first amplifier after the antenna contributes most to the system noise figure. Adding gain in front of a noisy network reduces the noise contribution from that network. So low noise amplifier (LNA) is encouraged to obtain a better gain.

Different LNA designs have different gain, NF, linearity and power consumption. To compare such designs, typically the multitude of LNA specifications are mappedinto a single scalar called figure of merit and its large value indicates a more efficientdesign. In the proposed work, a LNA at 2.4 GHz with matchingnetwork and improvedstability performance is to be designedand its performanceanalysis is simulated by using ADS.

II. RELATED WORK

A concurrent dual-band low-noise amplifier (LNA) targeted for W-LAN IEEE 802.11 a/b/g standards is designed using 0.13- m CMOS process. [1] To attain the power-constrained simultaneous noise and input matching at 2.4 and 5.2 GHz, cascode common source inductive degeneration topology is adopted. The LNA achieves input reflection coefficients of 16.8 and 19.4 dB, forward gains of 19.3 and 17.5 dB at 2.4 and 5.2 GHz, respectively. Furthermore, the LNA exhibits noise figures of 3.2 and 3.3 dB with input 1-dB compression points of 29.6 and 28.2 dBm, while third-order input intercept points of 20.1 and 18.1 dBm at 2.4 and 5.2 GHz, respectively. The LNA dissipates 2.4 mW of power from a 1.2-V supply.

A low power, high gain, optimized CMOS low noise amplifier (LNA) is presented in this paper intended for Bluetooth applications.[2]Employing CMOS Inverter as a core of the proposed LNA, the extra voltage gain within the low-power consumption is obtained. By improving the previous works on CMOS LNA optimization, we attain a comprehensive and compatible method to optimize the fundamental features of the CMOS Inverter Current Reused (CICR) family. The provided CICR LNA results inclusively prove the advantages of our design over other published topologies. The designed LNA based on 0.13µm CMOS technology demonstrates a 28.5dB voltage gain (S21), 2.4dB noise figure (NF), -18dB impedancematching (S11), and dissipating power less than 1mW at 2.4GHz frequency.

[3] An adaptive substrate (body) bias design for variability and reliability for a CMOS low-noise amplifier (LNA) is analyzed. The proposedbody biasing scheme provides a radio-frequency circuit that is resilient to*process variations and device reliability. Small-signal*models including substrate

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bias effect are developed for noise figure and small-signal power gain sensitivity. The cascode LNA operating at 2.4 GHz with the adaptive substrate bias scheme is compared with the LNA without body bias using the PTM 65nm technology. The modeling and simulation results show that the adaptive substrate bias reduces the sensitivity of noise figure and minimum noise figure subject to process variations and device aging such as threshold voltage shift and electron mobility degradation.

[4] This paper presents a technique using current-mode approach for a CMOS differential low noise amplifier design, simulated with a TSMC 0.18μm RF CMOS process, working at 1.2V supply. A comparison with conventional voltage-mode LNA shows that this LNA has advantages of low voltage, low power consumption and simple structure. Simulation results demonstrates that at 2.4Ghz, the noise figure is only 1.47 dB, transconductance gain is 12.63 dB, S11 is -26.47 dB, S22 is -23.64 dB. With Voltage of 1.2V, the power consumption is 6.49 mW.

III. PROPOSED WORK

Selection of the transistor is the crucial stage in LNA design. Each transistor has its maximum available gain (MAG)and minimum intrinsic noise figure (NFmin) at particular frequency. So a LNA which gives more gain than MAG and Noise figure less than NFmin cannot be designed. ATF-21170 transistors selected for LNA design as it is having values as per our targeted values.

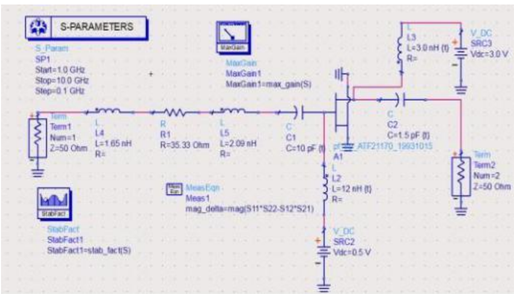

Fig. 1. Circuit Diagram of Low Noise Amplifier

The proper flow of Zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as Transistor biasing. The circuit which provides transistor biasing is called biasing circuit. The LNA is designed in the workspace of the ADS in the Standard ADS Layers, 0.0001millimeter layout resolutionby placing the lumped components from the component palette present in the left side of the ADS workspace. There are different categories to know about the stabilitysystem K >1 and <1 → unconditionally of the transistor. K< 1 and <1 → potentially stablestable system. For calculating thevalues of K and the following equation is used.

Depending on the values of S-Parameter, the values of K= 0.719obtained using ADS software and = 0.537. This shows that the value of K < 1 and < 1, this results in potential unstable transistor. The impedance matching network is implemented using the Z-Y plot available in the ADS. The inductance and resistor combination provides the impedance matching in the input port. Thus, the effect of impedance mismatch is overcome using this RL filter. Thus, the stability of the LNA is achieved by introducing matching network in the input port. Similarly, the impedance matching and stability can also be achieved by using other techniques as well.

IV. RESULTS

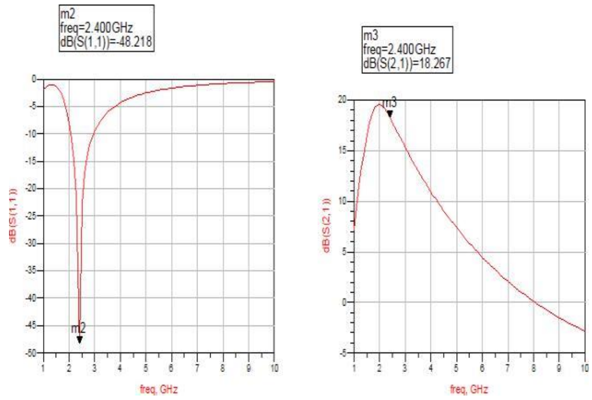

Fig. 2. S11 and S21 plots

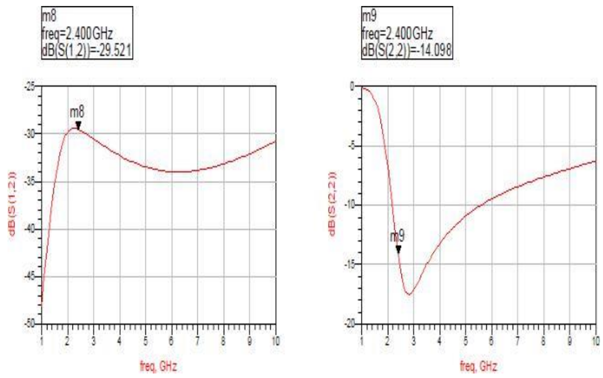

Fig. 3. S12 and S22 plots

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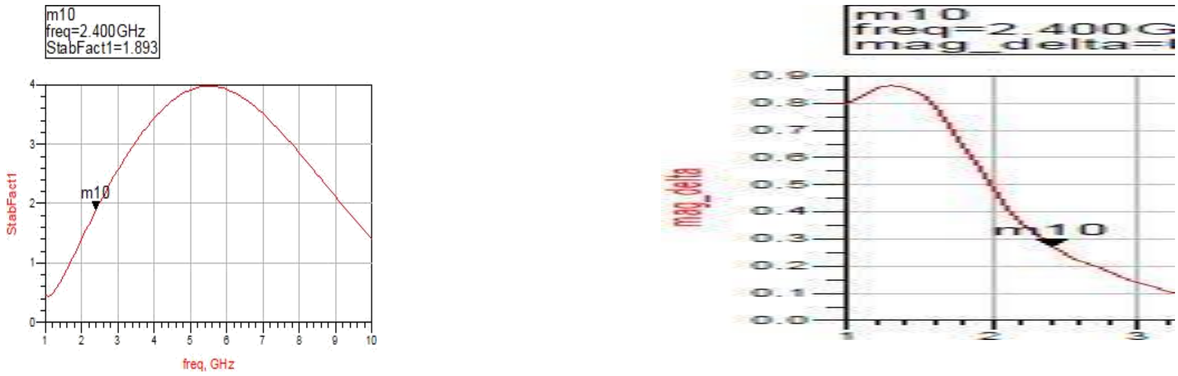

Fig. 4. Stability Factor Plot and Rowlett Factor Plot

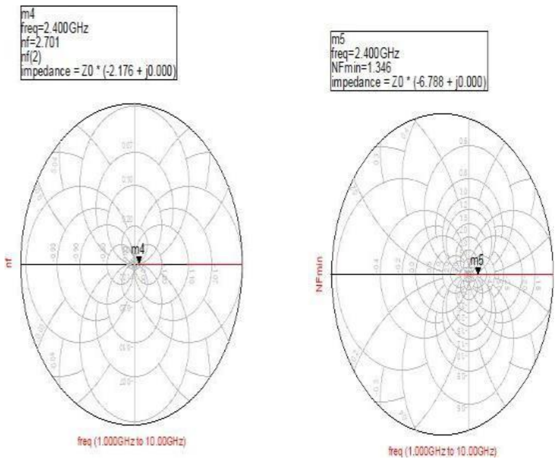

Fig. 5. Noise Figure and Minimum Noise Figure

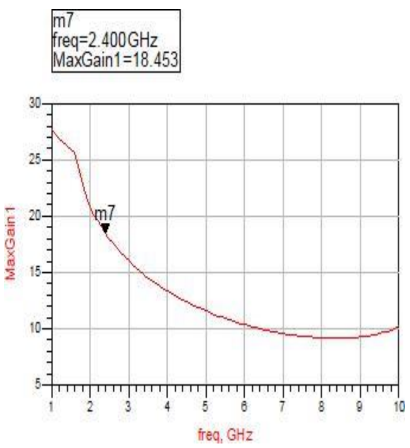

Fig. 6. Maximum Gain Plot

In Fig 2, the plot shows Input Voltage Reflection Coefficient, S11 = -48.218 dB, Forward Voltage Gain, S21 = 18.267 dB. In Fig 3, the plot shows Reverse Voltage Gain, S12 = -29.521 dB, Output Voltage Reflection Coefficient, S22 = -14.098 dB. In Fig 4, the plot shows Stability Factor =1.893 and Rowlett Factor = 0.274. In Fig 5, the plot shows Noise Figure = 2.701 Minimum Noise Figure, NFmin = 1.346. In Fig 6, the plot shows Maximum Gain = 18.453 dB

V. CONCLUSIONS

Though the responses are satisfactory, but still there are scopes to improve the performances. Some of the circuits can be improved in design and with more proper optimization to have better responses. [7]In future, different classes of BPFs such as elliptical, Chebyshev with different orders can be designed with LNA which will provide more options to compare for the better one. Furthermore, exact values of components which were used in the designs can be purchased and made new prototypes, which mayproduce better responses of LNA (designed with lumped components). However, the acquired knowledge from this work can help to design the whole RF receiver system in the ISM band

Hence the work performed pre and post layout simulation to validateproposed LNAs design. The fabrication of passive inductor requires larger silicon areaand it is not scalable as technology scale. Various activeinductor designtechniques arespecified in literature. [7]Activeinductor based

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LNA design requires less silicon area and design is scalable but it adds more noise and consumes more power compared to passive inductor design. The NF and power consumption of active inductor based LNA can be reduce by using noise cancelling and low power LNA design. RF frontend have three main analog blocks LNA, Mixer and Local oscillator. [7]The work is expand by the design of mixer and local oscillator for multi standard universal receiver and integrate proposed LNA design with mixer and local to make complete RF frontend.

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